Revision History.

Rev.	Date	Details
A	December 20, 2004	New release

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16MB to 8GB IDE Flash Drive

1.0 General Description

1.1 Overview

The IDE Flash Drive brings power of data portability to PC computing. It provides low power, high capacity mass storage in a IDE form factor and works like a hard drive, but has the speed and transportability of solid state devices.

These Drives are rugged, reliable and IDE compatible. They are available in 16MB, 32MB, 64MB, 128MB, 256MB, 512MB, 1GB, 2GB, 4GB, and 8GB capacities that are removable like floppy drives, but operate faster than hard disks.

Since there are no moving parts IDE Flash Drives provide reliable operation in conditions that can be normally hostile to hard disk drives.

These Drives operate at both 3.3V and 5.0V. This lower operating voltage compared to that of the hard drives means significantly less operating current, with lower heat dissipation, while avoiding the high current requirements of hard drive start-ups. Consequently overall throughput and productivity is increased.

Our IDE Flash Drives are designed with an integrated controller chip and special proprietary space-management architecture to maximize read/write operations. This eliminates the firmware delays associated with sector read and write functions found in first generation flash Drives. These Drives are available for various applications such as Consumer devices supporting a variety of embedded and industrial applications, PC Desktop and Servers.

1.2 Features

- 100% compatibility with IDE (PC/AT) interface for seemless incorporation in most embedded platforms
- 16MB to 8GB Capacities
- 512 byte block size
- Low power consumption - operates at both 5.0V and 3.3V
- Supports both 8 and 16 bit Data Register Transfers
- Write/Erase endurance $1x10^6$ cycles
- Internal ECC
- Minimum 10 years data retention time
- Industry standard metal enclosure

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1.3 Ordering Information

SMART Part Number	Chip Density	Physical Capacity	Sector Card	Head	Cylinder	Sector Track	Formatted Capacity
SM9FLAD2BE16J8x	128Mb	16MB	31,232	4	244	32	15,876,096
SM9FLAD2BE32J6x	256Mb	32MB	62,464	4	488	32	31,819,776
SM9FLAD2BE64J5x	512Mb	64MB	125,952	4	984	32	64,262,144
SM9FLAD2BE128D1x	1Gb	128MB	251,904	8	984	32	128,557,056
SM9FLAD2BE256N2x	2Gb	256MB	503,808	16	984	32	257,400,832
SM9FLAD2BE512N2x	2Gb	512MB	1,001,952	16	994	63	512,180,224
SM9FLAD2BE1024N2x	2Gb	1GB	2,014,992	16	1999	63	1,030,848,512
SM9FLAD2BE512N4x	4Gb	512MB	1,001,952	16	994	63	512,180,224
SM9FLAD2BE1024N4x	4Gb	1GB	2,014,992	16	1999	63	1,030,848,512
SM9FLAD2BE2048N4x	4Gb	2GB	4,029,984	16	3998	63	2,062,516,224
SM9FLAD2BE1024N9x	8Gb	1GB	2,014,992	16	1999	63	1,030,848,512
SM9FLAD2BE2048N9x	8Gb	2GB	4,029,984	16	3998	63	2,062,516,224
SM9FLAD2BE4096N4x	8Gb	4GB	8,053,920	16	7990	63	4,115,001,344
SM9FLAD2BE8192N9x	8Gb	8GB	16,128,000	16	16000	63	8,233,807,872

X: Operating Temperature Range

Blank - Commercial 0º C to +70º C

I - Industrial -40º C to + 85º C (Ref. to section 7.0.2, on page 62)

SM 9 FLA D2A E 1024 M 1 _

- SM — SMART Modular
- 9 — Memory Cards
- FLA — ATA Flash
- D2A — Product Type
  - M2A: Flash Disk * Mini-IDE
  - M2B: Flash Disk * Female 2.5" Mini- IDE
  - D1A: Flash Disk * 1.8" HDD FF with enclosure
  - D2B: Flash Disk * 2.5" HDD FF with enclosure
  - D3A: Flash Disk * 3.5" HDD FF with enclosure
  - M3A: Flash Disk * 40 pin Mini-IDE
- E — Interface
  - E: IDE - ATA-2 - PIO Mode 4
- 1024 — Disk Density
  - 16: 16MB
  - 32: 32MB
  - 64: 64MB
  - 128: 128MB
  - 256: 256MB
  - 512: 512MB
  - 1024: 1024MB
  - 2048: 2048MB
  - 4096: 4096MB
- M — ATA Ctlr
  - M: Storm BM
  - J: Twister AJ
  - D: Twister ALA
  - N: Storm BN
- 1 — Device Density
  - 8: 128Mb
  - 6: 256Mb
  - 5: 512Mb
  - 1: 1Gb
  - 2: 2Gb
  - 4: 4Gb
  - 9: 8Gb
- _ — Operating Temperature Range
  - Blank: Commercial 0-70ºC
  - I: Industrial -40 - +85ºC

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1.4 Specification Overview

1.4.1 Transfer Rates.

• Write Data Transfer Rate (Host to Flash)	6MB/sec (Capacity 128MB+) 3.6MB/sec (Capacity 64MB) 1.2MB/sec (Capacity <64MB)
• Host Interface Transfer Rate	16MB/s (burst with PIO Mode 4)
• Start-up Time (Sleep to Read/Write)	<10mS

1.4.2 Reliability.

• MTBF	>1,000,000 hours
• Data reliability	1 in 10^{14} bits, read
• Endurance	> 2,000,000 erase/program cycles

1.4.3 Power Requirements

• VCC	5.0V±10%	3.3V±5%
• Read	75mA(max)	45mA(max)
• Write	85mA(max)	55mA(max)
•		

1.4.4 Environmental Characteristics

• Shock	50G max. @ 11mS
• Vibration	15G peak to peak
• Operating temperature	0ºC to +70ºC (Commercial) -40º C to +85º C (Industrial)
• Storage temperature	-65ºC to +150ºC
• Humidity	5% to 95%
• Altitude	up to 80,000 ft.

1.4.5 Physical Dimensions

With Metal Enclosure

• Length	3.947 in. (100.25 mm.)
• Width	2.752 in. (69.90 mm.)
• Height	0.240 in. (6.10 mm)

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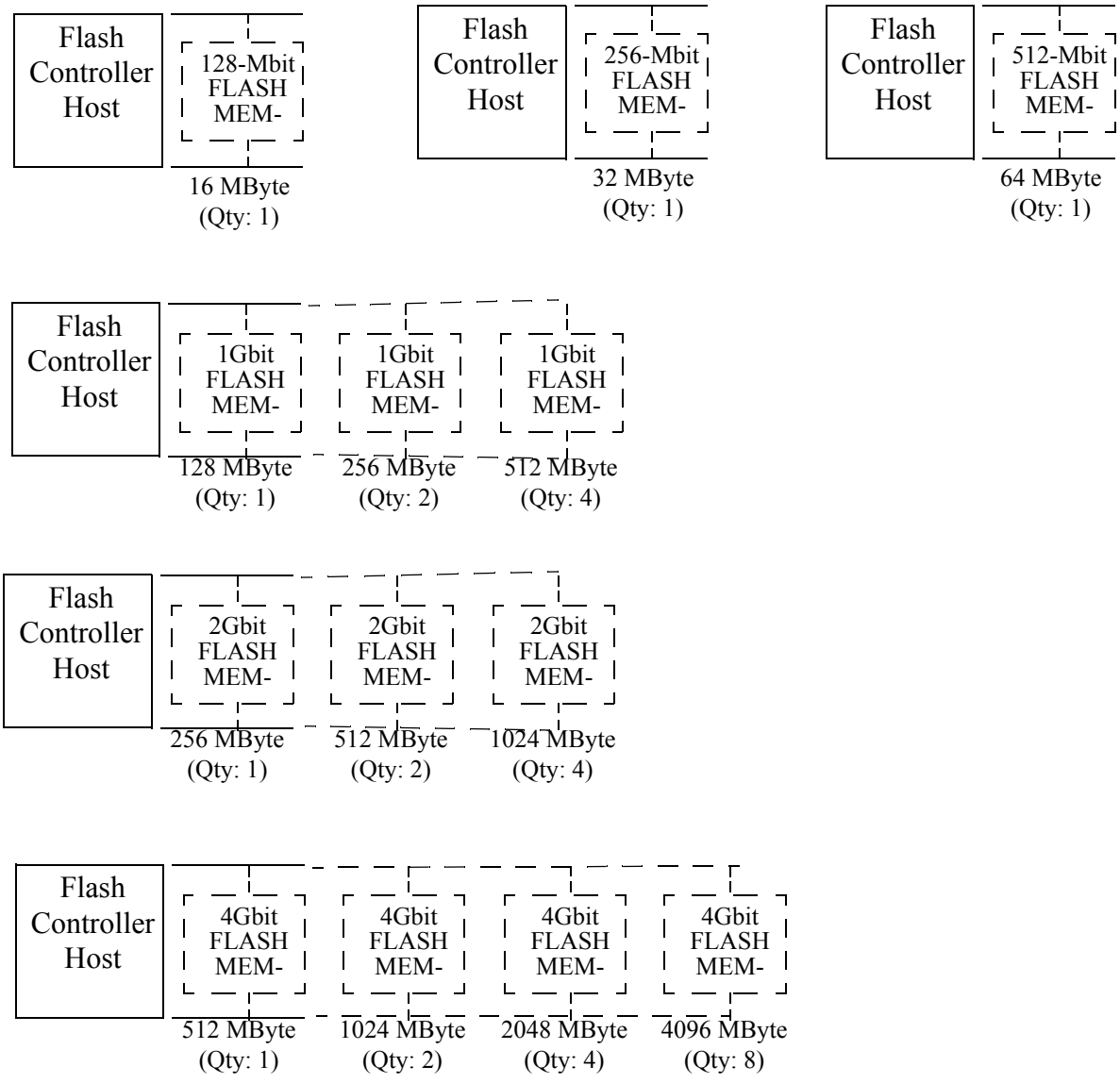
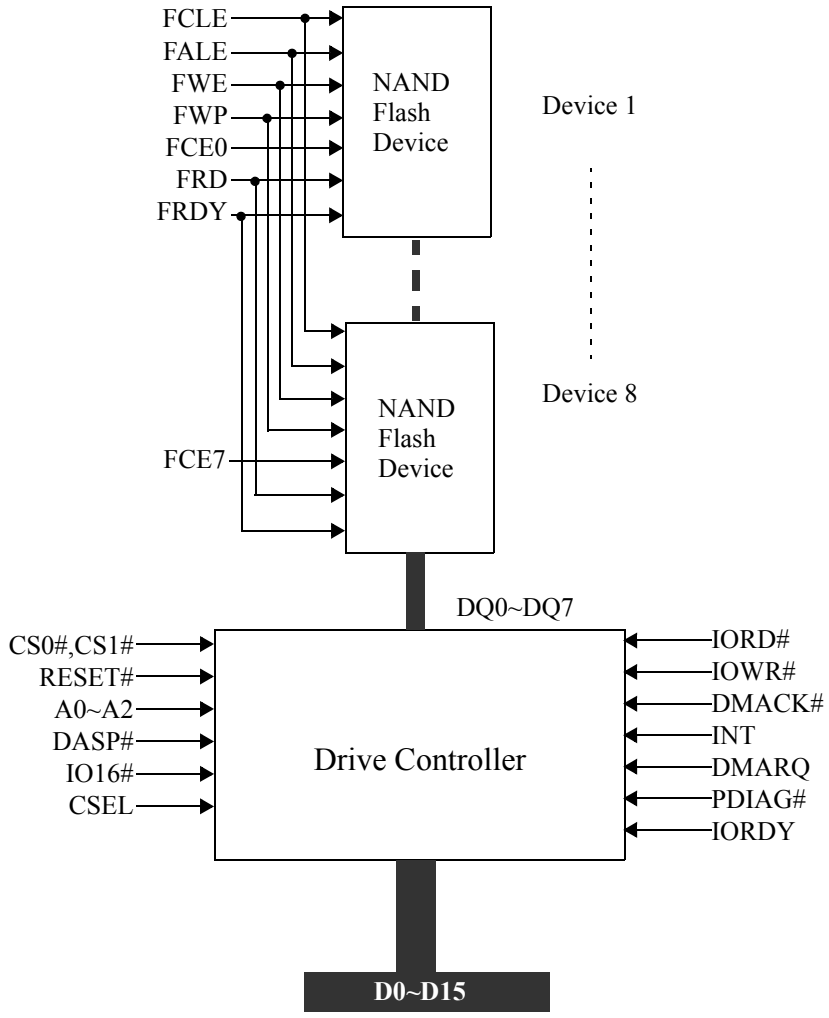
2.0 Module Block Diagram

The IDE Flash Drive contains a ATA/IDE controller and flash memory devices in a 44-pin connector. The controller interfaces with a host system allowing data to be written to and read from the flash memory devices.



2.1 Functional Block Diagram

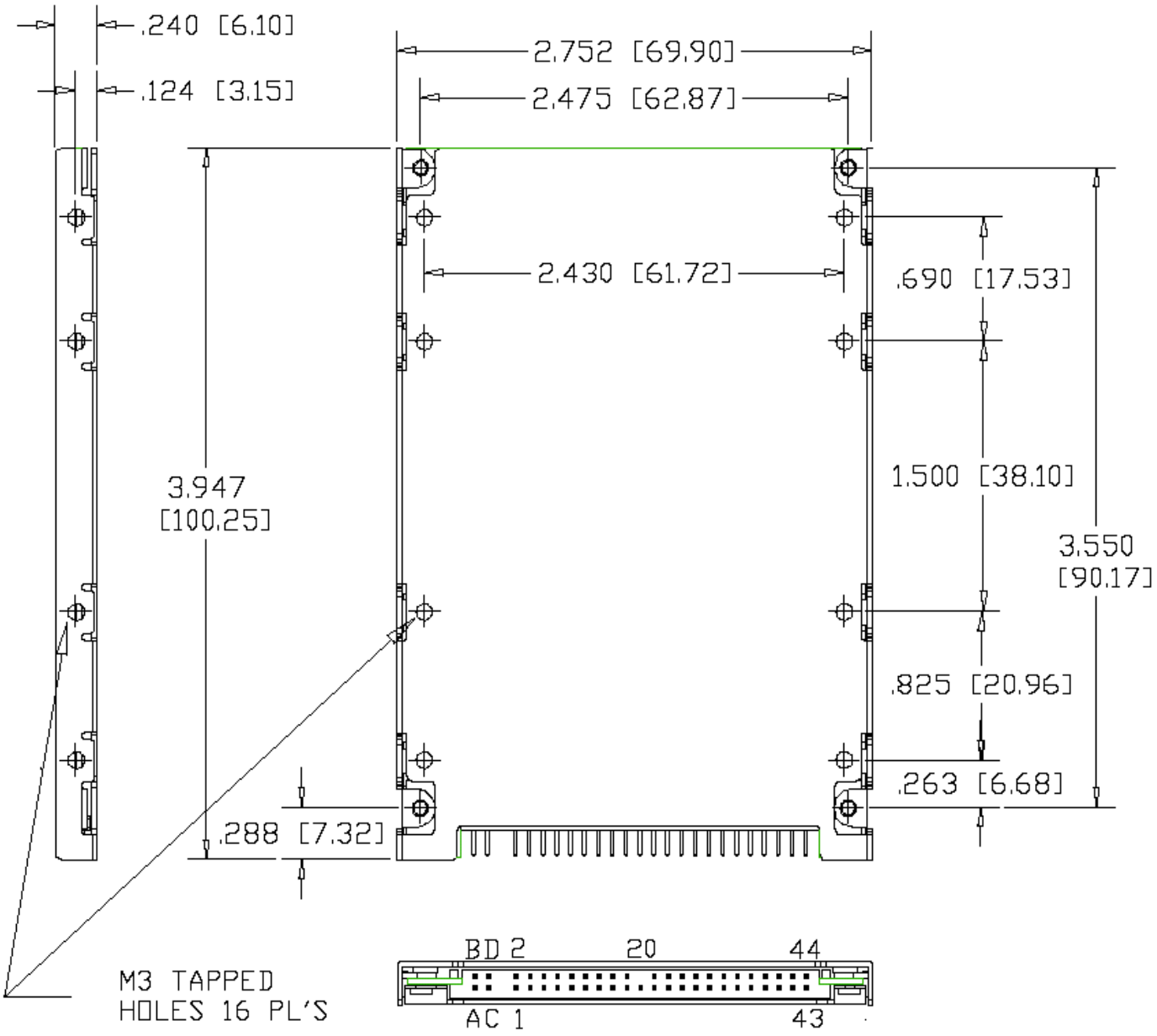


Notes :

1. All the signals shown going to the flash devices come from the IDE Drive controller. All the other signals including those going to the Drive controller come from the Drive Interface.
2. DMACK# and DMARQ have a 100K pull-up resistor.

2.2 Mechanical Specifications (continued)

Enclosure Option B - with metal enclosure



3.0 Electrical Interface

3.1 Electrical Description

The Flash IDE Drives are fully compliant with the ATA specification.

Table 1 describes the I/O signals. Signals whose source is the host are designated as inputs (I) while signals that the IDE Flash Drive sources are outputs (O). Bidirectional signals are designated as Input/Output (I/O).

Table 1. Pin Assignments and Pin Type

A. 44-Pin Connector

True IDE Mode			True IDE Mode		
Pin No.	**Signal Name**	**Pin Type**	**Pin No.**	**Signal Name**	**Pin Type**
1	RESET#	I	2	GND	Ground
3	DQ7	I/O	4	DQ8	I/O
5	DQ6	I/O	6	DQ9	I/O
7	DQ5	I/O	8	DQ10	I/O
9	DQ4	I/O	10	DQ11	I/O
11	DQ3	I/O	12	DQ12	I/O
13	DQ2	I/O	14	DQ13	I/O
15	DQ1	I/O	16	DQ14	I/O
17	DQ0	I/O	18	DQ15	I/O
19	GND	Ground	20	KEY	
21	DMARQ	O	22	GND	Ground
23	IOWR#	I	24	GND	Ground
25	IORD#	I	26	GND	Ground
27	IORDY	O	28	CSEL	I
29	DMACK#	I	30	GND	Ground
31	INTRQ	O	32	IO16#	O
33	A1	I	34	PDIAG#	I/O
35	A0	I	36	A2	I
37	CS0#	I	38	CS1#	I
39	DASP#	I/O	40	GND	Ground
41	VCC	Power	42	VCC	Power
43	GND	Ground	44	NC	

B. 6-Pin Drive Jumper Table

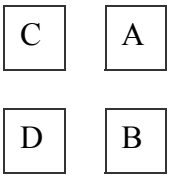
Pin No.	Signal Name	Pin No.	Signal Name
A	GND	B	S#/M
C	NC	D	CSEL
E	KEY	F	KEY

Note:

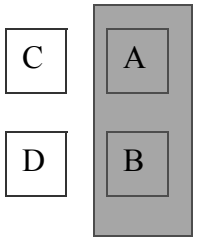
1. S#/M indicates that when pin "A" is grounded, the drive is configured as Slave and when pulled high, the drive is configured as Master.

2. Pins 20, E and F are keys and hence removed from the connector. See mechanical Specifications (Section 2.2. page 6).

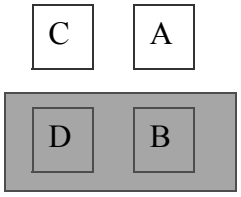
Drive Jumper Settings:



No Jumper: Master (Default)



Jumper A_B: Slave



Jumper B_D: Cable Select

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Table 2. Signal Description

Signal Name	Pin Type	Pin No(s).	Description
IOWR#	I	23	I/O Write Input
			The I/O Write strobe pulse is used to clock I/O data on the Drive data bus into the controller registers. The clocking will occur on the negative to positive going edge of the signa
IORD#	I	25	I/O Read Input
			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Drive.
CSEL	I	39	Cable Select Input
			This signal is used to configure this device as Master or Slave. When this pin is grounded, this device is configured as Slave. When this pin is tied to VCC this Drive is configured as Master.
CS0#, CS1#	I	37, 38	Chip Select Input
			CS0# is the chip select for the ATA Command block registers while CS1# is used to select the ATA Control Block registers (Alternate Status Register and the Device Control Registers).
IO16#	O	32	I/O Port 16 Output
			This signal is asserted low when the Drive is expecting a word data transfer cycle. This open collector line is only driven on assertion (low).
GND	Power	2, 19, 23, 24, 26, 30, 40, 43	Ground Pin
VCC	Power	41, 42	Power Supply Pin (5.0V/3.3V)
RESET#	I	1	Drive Reset Input
			This input pin is the active low from the host.
DQ0~DQ15	I/O	17, 15, 13, 11, 9, 7, 5, 3, 4, 6, 8, 10, 12, 14, 16, 18	16-bit Data Input/Output Bus All register operations occur in byte mode on DQ7~DQ0, while all data transfers are word (16-bit) accesses.

Table 2. Signal Description (continued)

Signal Name	Pin Type	Pin No(s).	Description
A0~A2	I	35, 33, 36	In this mode, only A0~A2 are used to select one of the Control/Status registers.
INTRQ	O	31	Interrupt Request Output
			This mode, the signal is active high request to the host.
DMARQ	O	21	DMA Request
			This signal which is used as the DMA Request signal in the ATA/IDE Specifications is not used in this Drive and is connected to VCC.
IORDY	O	27	I/O Channel Ready Output
			This signal is held low to extend the host transfer cycle of any host register access (read or write) when the Drive is not ready to respond to a data transfer request.
PDIAG#	I/O	34	Passed Diagnostics
			This signal is asserted by slave drive to indicate to master drive that it has completed diagnostics and is ready to provide status.
DASP#	I/O	39	Device Active/Slave Present Input/Output
			This signal indicates that a drive is active or that a slave drive (Drive 1) is present.
DMACK#	I	29	DMA Acknowledge
			This signal which is used by the host as DMA Acknowledge is not used in this drive and is tied to V_{CC}.

4.0 FLASH Drive Register Set Definition

In the True IDE Mode the Drive protocol and configuration are disabled and only I/O operations to the task file and Data Registers are allowed.

4.1 FLASH Drive Truth Table

CE2#	CE1#	A2~A0	IORD#	IOWR#	D15~D8	D7~D0	Function Mode
0	0	X	X	X	High Z	High Z	Invalid
1	1	X	X	X	High Z	High Z	Standby Mode
1	0	1-7h	1	0	XX	Data In	Task File Write
1	0	1-7h	0	1	High Z	Data Out	Task File Read
1	0	0	1	0	Odd Byte in	Even Byte in	Data Register Write
1	0	0	0	1	Odd Byte out	Even Byte out	Data Register Read
0	1	6h	1	0	XX	Control In	Control Register Write
0	1	6h	0	1	High Z	Status Out	All Status Read

4.2 Task File Register Addressing

CE2#	CE1#	A2	A1	A0	IORD# = 0	IOWR# = 0
1	0	0	0	0	Even RD Data	Even WR Data
1	0	0	0	1	Error	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Drive/Head	Select Drive/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Drive Control
0	1	1	1	1	Drive Address	Reserved

4.3 ATA Registers

4.3.1 Error Register

This register contains additional information about the source of an error when as error is indicated in bit 0 of the Status Register. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15~D8 during a write operation to offset 0 with CE2# low and CE1# high.

Bit 7 (BBK)	This bit is set when a Bad Block is detected. This bit is set when Error on Drive 1 (True IDE).
Bit 6 (UNC)	This bit is set when an Uncorrectable Read Error is encountered.
Bit 5	This bit is set to 0.
Bit 4 (IDNF)	The requested sector ID is in error or cannot be found.
Bit 3	This bit is set to 0.
Bit 2 (ABRT)	This bit is set if the command has been aborted because Drive status: Not Ready, Write Fault, or when an invalid command has been issued.
Bit 1	This bit is set to 0.
Bit 0 (AMNF)	This bit is set in case of a general error.

4.3.2 Feature Register

This register provides information regarding features of the Drive that the host can utilize.

4.3.3 Sector Count Register

This register contains the number of sector.s of data requested to be transferred on a read or write operation between the host and the PC Drive. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred to complete the request.

4.3.4 Sector Number (LBA 7~0) Register

This register contains starting sector number or bits 7~0 of the Logical Block Address (LBA) for any Drive data access for the subsequent command.

4.3.5 Cylinder Low (LBA 15~8) Register

This register contains the low order 8 bits of the starting cylinder address or bits15~8 of the Logical Block Address (LBA).

4.3.6 Cylinder High (LBA 23~16) Register

This register contains the high order 8 bits of the starting cylinder address or bits 23~16 of the Logical Block Address (LBA).

4.3.7 Drive/Head (LBA 27~24) Register

The Drive/Head register is used to select the drive and head. It is also used to select the LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7	This bit is set to 1.
Bit 6 (LBA)	LBA is a flag to select either cylinder/head/sector (CHS) or LBA Mode. When this bit is zero, CHS mode is selected. When this bit is one, LBA mode is selected. In LBA Mode, the LBA is interpreted as follows: LBA7~LBA0: Sector Number Register D7~D0 LBA15~LBA8: Sector Number Register D7~D0 LBA23~LBA16: Sector Number Register D7~D0 LBA27~LBA24: Sector Number Register HS3~HS0
Bit 5	This bit is set to 1.
Bit 4 (DRV)	DRV is the drive number. When DRV is zero, drive/Drive 0 is selected. When DRV is one, drive/Drive 1 is selected. The Drive is set to be Drive 0 or 1 using the copy field (Drive#) of the Drive Socket & Copy configuration register.
Bit 3 (HS3)	When operating in the CHS mode, this is bit 3 of the head number. It is Bit 27 when in LBA mode.
Bit 2 (HS2)	When operating in the CHS mode, this is bit 2 of the head number. It is Bit 26 when in LBA mode.
Bit 1 (HS1)	When operating in the CHS mode, this is bit 1 of the head number. It is Bit 25 when in LBA mode.
Bit 0 (HS0)	When operating in the CHS mode, this is bit 0 of the head number. It is Bit 24 when in LBA mode.

4.3.8 Status & Alternate Status Register

This register returns the Drive status when read by the host. Reading the status register does clear a pending interrupt while reading the alternate status register does not. The status and alternate status registers are read only registers. When writing to the address of the status register command register is written. When writing to the address of the alternate status register, device control register is written. The status bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (Busy)	When the busy bit is set, the controller is executing a command. Also, when this bit is set, the host may not read or write any other register except the Status, Alternate Status, Device Control, or Drive Address registers. This bit is set when RESET# is asserted. It is also set when an AT host sets Device Control Register, Bit 2 or when the Command registers is loaded by the host.
Bit 6 (RDY)	RDY indicated whether the device is capable of performing Drive operations. This bit is cleared at power up and remains cleared until the Drive is ready to accept a command.
Bit 5 (DWF)	This bit, if set, indicates a write fault has occurred.
Bit 4 (DSC)	This bit is set when the Drive is ready. This bit is cleared at power up.
Bit 3 (DRQ)	The bit is set when the Drive requires that information be transferred either to or from the host through the data register.
Bit 2 (CORR)	This bit is set when a correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation. This bit is cleared when the Command register is written.
Bit 1 (0)	This bit is always set to 0.
Bit 0 (ERR)	This bit is set when the previous command has ended in some type of error. The bits in the error register contain additional information describing the error. This bit is cleared when the Command register is written.

4.3.9 Device Control Register

This register is used to control the Drive interrupt request and to issue an ATA soft reset to the Drive. This register can be written even if the Drive is BUSY. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	HD3En	SW Rst	IEn#	DMAEN

Bit 7 ~ Bit 4	These bits are don't care. But it is recommended that the user program these bits to zero.
HD3En	This bit is set to enable bit 3 of the address of the selected drive head giving a 4-bit addressable range corresponding to 1 to 16 heads.
Bit 2 (SW Rst)	This bit is set to one in order to force the Drive to perform an AT Disk controller soft reset operation. This does not change the Drive configuration registers as hardware reset does. The Drive remains in reset until this bit is reset to zero.
Bit 1 (IEn#)	The interrupt enable bit enables interrupts when the bit is zero. When this bit is set to one interrupts from the Drive are disabled. This bit also controls the Int bit in the configuration and status register. This bit is set to one at power on and reset.
DMAEN	The DMA Enable bit is an extra feature that this Drive supports for AT, that is not a generic AT interface. This feature allows a DMA channel to be multiplexed between multiple peripherals directly by the PC without local micro controller help. To enable this feature, the DMA mode must be selected in the Host Mode Control Register (Register 58H, bit 3), and the enable DMA control must be sent in the Misc. Control/Status Register (Register 52H, bit 4). With these two control bits set, the Device Control register bit 0 controls the DMA Enable of the DMA channel.

4.3.10 Drive Address Register

This is a diagnostic loop back register that contains Write Gate, Head Select3/Reduced Write Current, Head Select 2, Head Select 1, Head Select 0, Drive Select Drive 1, and Drive Select Drive 0. These bits reflect the state of the signals on the control cable. The host may read this register at any time. When host reads this register, only bits 6:0 are driven, bit 7 is High Impedance. NOTE: The Drive Address Register, also referred to as the Digital Input Register, is no longer supported in the ATA specifications. However, for backward compatibility, the Compact Flash Drives still supports this register, and responds as described.

B7	B6	B5	B4	B3	B2	B1	B0
HiZ	Wgate	H3/RWC	H2	H1	H0	DS1	DS0

5.0 ATA Command Description

This section documents the Host Interface Commands supported by the IDE Drive Controller. Two standard classes of interface specifications are currently implemented: the AT Attachment interface specifications, and the ATA specifications when operating in the true IDE mode.

Each command is discussed in terms of the contents of the Task File when the command is issued, the contents of the Task File when the host read the status after the command is completed, as well as the data that is transferred in response to the command issued.

5.1 ATA Command Set

The table below summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

ATA Specification type	Command	Code
O	Check Power Mode	E5h or 98h
M	Executive Drive Diagnostic	90h
V	Erase Sector(s)	C0h
M	Format Track	50h
O	Identify Drive	ECh
O	Idle	E3h or 97h
O	Idle Immediate	E1h or 95h
M	Initialize Drive Parameters	91h
O	Read Buffer	E4h
O	Read DMA	C8h
M	Read Long Sector	22h or 23h
O	Read Multiple	C4h
M	Read Sector(s)	21h or 21h
M	Read Verify Sector(s)	40h or 41h
M	Recalibrate	1Xh
V	Request Sense	03h
M	Seek	7Xh
O	Set Features	EFh
O	Set Multiple Mode	C6h
O	Set Sleep Mode	E6h or 99h
O	Stand By	E2h or 96h
O	Stand By Immediate	E0h or 94h
V	Translate Sector	87h
V	Wear Level	F5h
O	Write Buffer	E8h
O	Write DMA	CAh
M	Write Long Sector	32h or 33h
O	Write Multiple	C5h
V	Write Multiple w/o Erase	CDh
M	Write Sector(s)	30h or 31h
V	Write Sector(s) w/o Erase	38h
O	Write Verify	3Ch

Note:
1. Type Abbreviation:
   - M - Mandatory Command
   - O - Optional Command
   - V - Vendor Unique Command
2. These type abbreviations pertain to the ATA Specifications only. In the case of Compact-Flash-ATA specifications, all Host commands listed here are Mandatory.

5.2 ATA Command Set Definition

This section details the functionality of commands supported by the Flash Drive. For each command, the Command Block register contents for the command invoked by the Host, and the Command Block registers updated by the Flash Drive after command completion, are shown. Following is an example of the command description, showing the conventions used for each command description. Throughout this document, the terms 'Task File' and 'Command Block' are used interchangeably to refer to the ATA I/O registers

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A detailed description of the execution of the command is provided. This is followed by two tables, the first showing the requirements of the Command Block registers at the time that the Host issues the command to the Flash Drive, and the second showing the contents of the Command Block after completion or termination on error of the command.

Command Block specified by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	Command Code							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	Set Features Code							

The preceding table represents the contents of the Command Block registers when the command is issued by the Host. Where applicable, the Host first writes the appropriate data into the Features, Sector Count, Sector Number, Cylinder Hi/Low, and Drive/Head registers, and lastly, writes the command code into the Command register. The act of writing to the command register causes the Flash Drive to execute the command based on the contents of the Command Block at that instance.

Note that bits 7 and 5 of the Drive/Head register are denoted as 'nu.' Although the Host is expected to always set these bits to 1 when the command is issued, the Flash Drive ignores the value of these bits.

Command Block specified by Flash Drive upon completion/termination of 'Sample' command								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	0	V	0	V	0	0

The above table represents the contents of the Command Block registers upon completion of the command by the Flash Drive.

At the completion of every command, specific bits in the Status register is as follows: the BuSY, DriveWriteFault, DataReQuest, and InDeX bits are always de-asserted, while the DriveReaDY, and DriveSeekComplete bits are always asserted. The CORRected ECC bit and the ERRor bit are set or cleared as appropriate.

The contents of the Error register are always set to zero when a command is received, and are only valid if the ERR bit in the Status register is set to '1' at the completion of a command. In addition, the MediaChange, MediaChangeRequest, TracK0NotFound, and AddressMarkNotFound bits are always cleared, regardless of the state of the ERR bit in the Status register.

For the Command Block tables, explanations for each possible code are shown below:

L (LBA Mode bit)	This bit is used to specify whether the requested sector is addressed in the LBA mode or in the Cylinder-Head-Sector, CHS, mode. When set, the LBA mode is specified. The LBA is comprised of the lower significant nibble in the Drive/Head register, LBA[27:24], concatenated with the contents of the Cylinder Hi/Lo, and the Sector registers, LBA[23:0], respectively. If L=0, the sector is addressed in the classic Cylinder/Head/Sector CHS mode.
D (Drive Select bit)	This bit is used to select Drive 0 or 1, allowing up to two Drives to share a single Task File. If two PC Drive ATA Drives are present in the system, one of the Drives may be assigned as copy 0, and the second Drive may be assigned as copy 1, using the Copy field of the PCMCIA Socket & Copy Drive configuration register. In this case, the Drive designated as Copy 0 is selected when D=0. Conversely, the Drive designated as Copy 1 is selected when D=1.
1 (Bit is Set)	When referring to the Command Block registers when the Host issues a command, this bit must be set to a 1 by the Host before command invocation. When referring to the Command Block contents read by the Host after completion of a command, this bit is set by the Flash Drive upon command completion.
0 (Bit is Cleared)	When referring to the Command Block registers when the Host issues a command, this bit must be cleared to 0 by the Host before command invocation. When referring to the Command Block contents read by the Host after completion of a command, this bit is cleared by the Flash Drive upon command completion.
nu (Not Used)	Although the Host may specify this register/bit when invoking the command, the value for this command block register or bit is ignored by the Drive.
V (Valid Data)	When referring to the Command Block contents read by the Host after completion of a command, the value for the applicable bit is specified by the Drive.
na (Not Affected)	The value for this bit, or register, is neither set nor cleared by the Drive; i.e., it is unchanged by the Drive after command completion.

5.2.1 Check Power Mode

Although this command is supported for backward compatibility, it has no actual function. The Drive always returns the In Idle mode code 'FFh' in the Sector Count register, in response to this command. Command completion status always indicates command completed with no error.

Check Power Mode Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h/E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Check Power Mode command (98h/E5h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	Power Mode Code is always FFh							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.2 Erase Sectors

This command erases the number of sectors specified in the Sector Count register, starting at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File.

Erase Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C0h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to eraser							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to eraser							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to erase							
SECTOR COUNT	The number of sectors/logical blocks to erase							
FEATURES	nu							

Command Block specified by Flash upon completion/termination of Erase Sectors command (C0h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	V	1	0	0	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector erased			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector erased							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector erased							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector erased							
SECTOR COUNT	The number of sectors that were not erased if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

5.2.3 Execute Drive Diagnostics

This command performs self-diagnostics on various internal components of the Flash Drive. Results of the test are reported in the Error register. Note that the bit definitions for the Error register do not apply in this command; rather, the value in the Error register is a diagnostic code, defined in the Table below.

Execute Drive Diagnostics Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Execute Drive Diagnostics command (90h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/ HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	Diagnostic Code. See Table below							

Execute Drive Diagnostic Return Codes	
Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC logic error
05h	Controller microprocessor error
8xh	Slave Error[a]

a. Valid only if Flash Drive is in True IDE Mode.

5.2.4 Format Track

This command erases 32 sectors starting at the sector specified by the Cylinder, Head, and Sector Number parameters in the task file. If the sector is not valid, an IDNF (ID Not Found) bit is set in the Error register and the command terminates.

In CHS mode, the number of sectors to format per track is set to the number of Current Sectors per Track in the Identify Drive data, by default 20h. Otherwise, it is set to the number of sectors per track as set by the Initialize Drive Parameters command.

In LBA mode, the number of sectors to format per track is specified by the Host in the Sector Count register. For backward compatibility, the Flash Drive accepts one sector of data from the Host. This data is not used.

Format Track Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	50h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	[LBA mode only] LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	[LBA mode only] The number of sectors to be formatted on the track.							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Format Track command (50h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

5.2.5 Identify Drive

This command passes to the Host one sector of data describing the Flash Drive's parameters. See Table for a detailed description of the Identify Drive data.

Identify Drive Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Identify Drive command (ECh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

Drive Information		
Word	Data	Description
0	045Ah	General configuration bit-significant information:
1	Note 1	Number of Cylinders
2	0000h	Reserved
3	Note 1	Number of Heads
4	4000h	Number of unformatted bytes per track
5	0200h	Number of unformatted bytes per sector
6	Note 1	Number of sectors per track
7-9	0000h 0000h 0000h	Vendor unique
10-19	XXXXh	20 ASCII char serial number. Words 10-19 are filled with 20 ASCII ‘space’ chars.
20	0002h	Buffer type: Dual ported, multi-sector, w/read cache

Drive information continued

Word	Data	Description
23-26	V1.xx	Firmware revision, 8 ASCII chars where xx is minor revision number
27-46	[Manufacturer's info]	Model number, 40 ASCII chars.
47	0004h	Maximum Block Count=1 for Read/write Multiple commands
48	0000h	Cannot perform double word I/O
49	0200h	Capabilities: LBA supported, DMA not supported
50	0000h	Reserved
51	0200h	PIO timing mode 2,
52	0000h	DMA transfer not supported
53	0003h	Words 54 - 58 are valid
54	Note 1	Number of Current Cylinders
55	Note 1	Number of Current Heads
56	Note 1	Number of Current Sectors Per Track
57	Note 1	LSW of the Current Capacity in Sectors
58	Note 1	MSW of the Current Capacity in Sectors
59	0001h	Current Setting for Block Count=1 for R/W Multiple commands
60-61	Note 1	LSW of the total number of user addressable LBA's
62-63	0000h	Reserved
64	0003h	Advanced PIO modes supported
65-66	0000h	Reserved
67	0078h	Minimum PIO transfer cycle time without flow control
68	0078h	Minimum PIO transfer cycle time with IORDY flow control
69-81	0000h	Reserved
82-84	0000h	Features/command sets supported

Drive information continued

88	0000h	Reserved
89	0000h	Time required for Security erase unit completion
90	0000h	Time required for Enhanced Security erase unit completion
91	0000h	Current Advanced power management value
92-127	0000h	Reserved
128	0000h	Security status
129-159	0000h	Vendor unique bytes
160	0000h	Power requirement description
161	0000h	Reserved for assignment by the CFA
162	0000h	Key management schemes supported
163-175	0000h	Reserved for assignment by the CFA
176-255	0000h	Reserved

Note 1: This value is dependent upon the total capacity of the specific flash Drive.

5.2.6 Idle

Although this command is supported for backward compatibility, it has no actual function. The Drive always returns good status at the completion of this command.

Idle Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h/E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Time-out Parameter. This parameter is ignored by the Drive.							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Idle command (97h/ E3h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

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5.2.7 Idle Immediate

Although this command is supported for backward compatibility, it has no actual function. The Drive always returns good status at the completion of this command.

Idle Immediate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h/E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Idle Immediate command (95h/E1h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

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5.2.8 Initialize Drive Parameter

This command allows the Host to alter the number of sectors per track and the number of heads per cylinder. This enables Translation Mode which maps the flash storage using the altered parameters. On Host Reset, the default is 32 Sectors per Track and 8 Heads per Cylinder. The current values used for mapping are returned in the Identify Drive command as Number of Current Sectors per Track, and Number of Current Heads.

Initialize Drive Parameters Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	91h							
DRIVE/HEAD	nu	nu	nu	D	Number of Heads per Cyl minus 1			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	The Number of Sectors per Track							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Initialize Drive Parameters command (91h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.9 Read Buffer

This command transfers the current contents of the first page of the data buffer (512 bytes) to the Host.

Read Buffer Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	E4h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Read Buffer command (E4h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.10 Read DMA

This command transfers data from the Flash card to the Host using DMA. The data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register.

Read DMA Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	1	LBA	1	Drive	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

5.2.11 Read Long

This command is similar to the Read Sectors command except the contents of the Sector Count register are ignored and only one sector is read. The 512 data bytes and 4 ECC bytes are read into the buffer (with no ECC correction) and then transferred to the Host.

Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	22h (retries enabled) -or- 23h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the sector/ LBA to trans fer			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer. This should be set to 01 for compatibility							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Read Long command (22h/23h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] of the sector requested			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector requested							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector requested							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the sector requested							
SECTOR COUNT	00 if the command proceeded without error. 01 if an error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

5.2.12 Read Multiple

The R/W Multiple commands have to be enabled by a previous valid Set Multiple command. Once enabled, the Read Multiple command is identical to Read Sectors operation, except that the number of sectors as specified in the most recent Set Multiple command are transferred as a block to the Host without intervening Host handshaking. This number of sectors to transfer as a block is referred to as the block count. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block count is one. If Read Multiple has not been enabled, the ABRT (Aborted Command) bit is set in the Error register and the command terminates.

Read Multiple Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
	C4h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Read Multiple command (C4h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred. Zero otherwise.							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

5.2.13 Read Sectors

This command transfers data from the Flash Drive to the Host. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register.

Read Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	20h (retries enabled) -or- 21h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Read Sectors command (20h/21h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

5.2.14 Read Verify Sectors

The Read Verify Sectors command verifies one or more sectors on the Drive by transferring data from the Flash media to the data buffer in the Drive and verifying that the ECC is correct. It is performed identically to the Read Sectors command, except that DRQ is not asserted, and no data is transferred to the Host. If an uncorrectable error occurs, the read verify is terminated at the failing sector. The Command Block registers contain the CHS, or LBA of the sector in which the error occurred.

Read Verify Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	40h (retries enabled) -or- 41h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to verify							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to verify							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to verify							
SECTOR COUNT	The number of sectors/logical blocks to verify							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Read Verify Sectors command (40h/41h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last sector verified, or sector where an unrecoverable error occurred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector verified, or sector where an unrecoverable error occurred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector verified, or sector where an unrecoverable error occurred							
SECTOR NUM	Sector or LBA[7:0] of the sector verified, or sector where an unrecoverable error occurred							
SECTOR COUNT	The number of sectors that were not yet verified if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

5.2.15 Recalibrate

Although this command is supported for backward compatibility, it has no actual function. The Drive always returns good status at the completion of this command.

Recalibrate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	1xh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Recalibrate command (1xh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.16 Request Sense

This command returns an extended error code for the previous command which ended with an error. Table below defines and describes the contents of the Error register on completion of the Request Sense command.

Request Sense Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	03h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Request Sense command 03h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	See Table below							

Extended Error Codes	
Extended Error Code	Description
00h	No error detected
01h	Self test OK (no error)
09h	Miscellaneous error
20h	Invalid command
21h	Invalid address (Requested Head or Sector invalid)
2Fh	Address overflow (Address too large)
35h, 36h	Supply or generated voltage out of tolerance
11h	Uncorrectable ECC error
18h	Corrected ECC error
05h, 30-34h, 37h, 3Eh	Self test or diagnostic failed
10h, 14h	ID not found
3Ah	Spare sectors exhausted
1Fh	Data transfer error/Aborted command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted media format
03h	Write/Erase failed

5.2.17 Seek

This command is supported for backward compatibility. Although this command has no actual function, it does perform a range check of valid track, and posts an IDNF error if the Head or Cylinder specified are out of bounds.

Seek Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	7xh							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the track			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the track							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the track							
SECTOR NUM	(Valid in LBA mode only) LBA[7:0] of the track							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Seek command (7xh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

5.2.18 Set Features

This command allows the Host to control various Drive features. Each feature is selected by passing its feature code in the Features register. Certain features use additional information passed in the Sector Count register. If the Feature register contains a feature code that is not supported, the drive will respond by setting the Error bit in the Status register and the Abort bit in the Error register.

Set Features Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	EFh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu (additional info if features code is 97h or 9Ah)							
FEATURES	Feature Code. See Table on page […]							

Command Block specified by Flash Drive upon completion/termination of Set Features command (EFh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na (8: maximum current divided by 4 if feature code is 9Ah)							
CYLINDER LOW	na (2: minimum current divided by 4 if feature code is 9Ah)							
SECTOR	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

Valid Feature Codes	
Code	Feature
01h	Enable 8-bit data transfers
44h	NOP; accepted for backward compatibility
55h	NOP; accepted for backward compatibility
66h	Disable restoration of default features with Soft Reset
69h	NOP; accepted for backward compatibility
81h	Disable 8-bit data transfer
96h	NOP; accepted for backward compatibility
97h	Control clock using value in Sector Count register
9Ah	Control current using value in Sector Count register
Aah	NOP; accepted for backward compatibility
BBh	NOP; accepted for backward compatibility
CCh	Enable restoration of default features with Soft Reset

NOTES

Feature codes 01h and 81h controls Host transfer data width. By default, 8-bit transfers are disabled.

Feature codes 44h, 55h, 69h, 96h, AAh, and BBh are supported for backward compatibility and have no function.

Feature codes 66h and CCh control whether or not a Soft Reset restores any feature codes to their Power On default value. The features effected are 81h (8-bit transfer), 97h (clock control), and 9A (current control). By default, a Soft Reset will restore the default features.

Feature codes 97h and 9Ah are used to control the Drive's power and performance. They are mutually exclusive; each feature code will overwrite the power/performance features set by the other command.

Feature code 97h controls the Drive's internal clock using the value set in the Sector Count register. See Table below. The default value is 0Fh.

Sector Count Code Specifying Flash Drive's Internal Clock Rate	
Sector Count Register Value	Function
00h	Lowest power/slowest performance
0Ah	Intermediate power and performance
0Bh	Intermediate power and performance
0Eh	Highest power/fastest performance
0Fh	Highest power/fastest performance

Feature code 9Ah enables the Drive to self-configure to best meet the Host system's power requirements. The Host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the Drive should consume. For example, if the Sector Count register is set to 6, the Drive will self-configure to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the Drive responds to the Host with the range of values supported by the Drive. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The Drive will accept values outside this programmable range, but will operate either at the lowest power or highest performance as appropriate.

5.2.19 Set Multiple

This command is used either to set the block count (number of sectors per block), simultaneously enabling R/W Multiple command support, or to disable support of R/W Multiple commands. Although setting, reading, and writing blocks are supported, the only valid block count is one. If the block count specified by the Host is greater than one, the command is aborted. The ERR bit in the Status register is set, and the ABRT bit in the Error register is set. In addition, Read Multiple and Write Multiple commands are disabled. If the contents of the Sector Count register is '1', Read Multiple and Write Multiple commands are enabled until the next Host RESET. Invoking this command with Sector Count = 0 disables R/W Multiple commands. In this case, all subsequent R/W Multiple commands issued by the Host are aborted by the Flash Drive.

Set Multiple Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C6h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	01: R/W Multiple command transfer enabled, 00: R/W Multiple command transfer disabled							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Set Multiple command (C6h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

5.2.20 Sleep

Although this command is supported for backward compatibility, it has no actual function. The Drive always returns good status at the completion of this command.

Sleep Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	99h/E6h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Sleep command (99h/E6h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.21 Standby

Although this command is supported for backward compatibility, it has no actual function. The Drive always returns good status at the completion of this command.

Standby Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	96h/E2h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Time-out Parameter. This is ignored by the Flash Drive							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Standby command (96h/E2h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.22 Standby Immediate

Although this command is supported for backward compatibility, it has no actual function. The Drive always returns good status at the completion of this command.

Standby Immediate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	94H/E0h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Standby Immediate command (94H/E0h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.23 Translate Sector

This command transfers one block of data to the Host relating to the sector specified in the Task File. See Table below for a detailed description of this data.

Translate Sector Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	87h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector/LBA							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Translate Sector command (87h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

Translate Sector Data Description	
Byte Address	Description
00h	00h
01h	Cylinder LSB
02h	Head
03h	Sector
04h-06h	LBA
07h-12h	00h
13h	Erased flag
14h-17h	00h
18h-1Ah	Hot Count (not supported)
1Bh-1FFh	00h

5.2.24 Wear Levelling

Although this command is supported for backward compatibility, it has no actual function. The Drive always returns good status at the completion of this command.

Wear Leveling Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Wear Leveling command (F5h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	00							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.25 Write Buffer

This command transfers 512 bytes of data from the Host to the first page of the data buffer.

Write Buffer Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	E8h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Write Buffer command (E8h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

5.2.26 Write DMA

This command transfers data from the Host to the Flash card. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register. If the address of the starting sector is not within the range of addresses supported by this card, the IDNF (ID Not Found)) bit is set in the Error register and the command terminates.

Write Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	CAh							
DRIVE/HEAD	1	LBA	1	Drive	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

5.2.27 Write Long

This command is similar to the Write Sectors command except the contents of the Sector Count register are ignored and only one sector is written. The 512 data bytes and 4 ECC bytes are transferred from the Host and then written from the buffer to the flash.

Write Long Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	32h (retries enabled) -or- 33h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer. Should be set to 1 for compatibility.							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Write Long command (32h/33h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	1 if an unrecoverable error occurred, 0 if the command proceeded successfully							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	V0

5.2.28 Write Multiple

The R/W Multiple commands have to be enabled by a previous valid Set Multiple command. Once enabled, the Write Multiple command is identical to Write Sectors operation, except that the number of sectors as specified in the most recent Set Multiple command are transferred as a block from the Host without intervening Host handshaking. This number of sectors to transfer as a block is referred to as the block count. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block count is one. If Write Multiple has not been enabled, the ABRT (Command Aborted) bit is set in the Error register and the command terminates.

Write Multiple Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C5h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Write Multiple command (C5h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

5.2.29 Write Multiple Without Erase

This command is supported for backward compatibility. The actual function performed is identical to the Write Multiple command.

Write Multiple without Erase Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	CDh							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Write Multiple without Erase command (CDh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

5.2.30 Write Sectors

This command transfers data from the Host to the Flash Drive. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register. If the address of the starting sector is not within the range of addresses supported by this Drive, the IDNF (ID Not Found)) bit is set in the Error register and the command terminates.

Write Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	30h (retries enabled) -or- 31h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Write Sectors command (30h/31h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

5.2.31 Write Sectors Without Erase

This command is supported for backward compatibility. The actual function performed is identical to the Write Sectors (with retry) command.

Write Sectors w/o Erase Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash Drive upon completion/termination of Write Sectors w/o Erase command (C8h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

5.2.32 Write Verify

This command is similar to the write sectors (without retry) command except that each sector is verified after being written.

Write Verify Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	3Ch							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

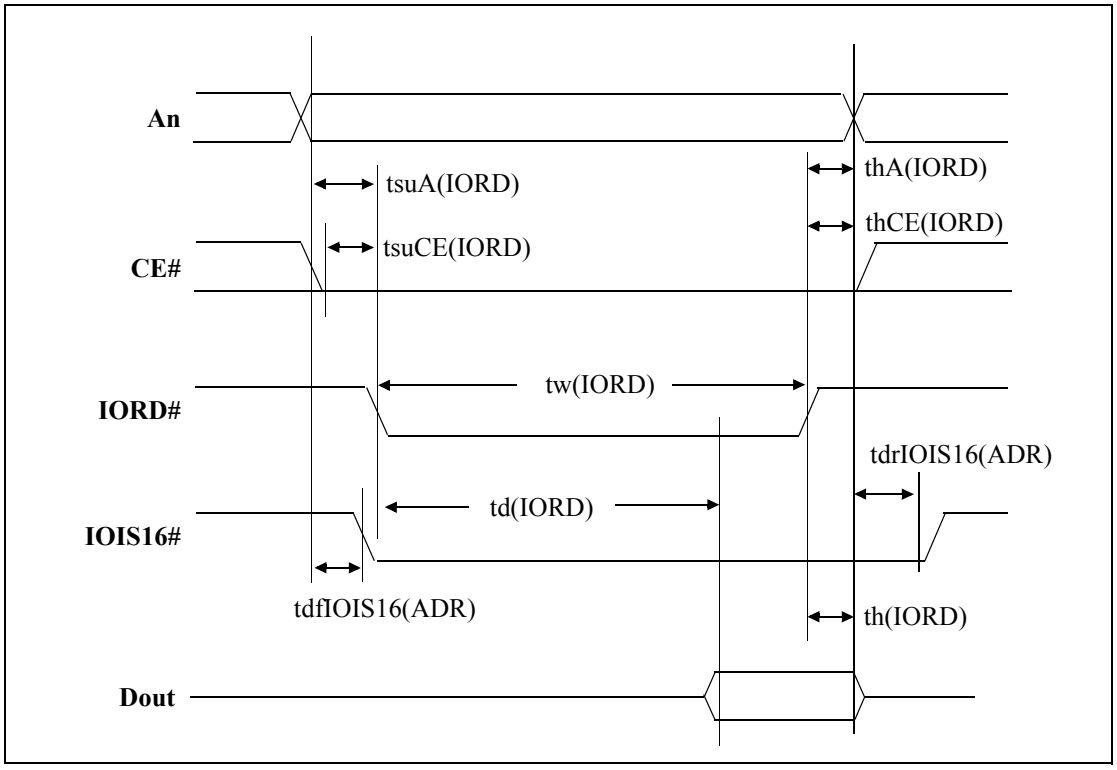
Command Block specified by Flash Drive upon completion/termination of Write Verify command (3Ch)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

6.0 Timing Diagrams

6.0.1 True IDE Mode Read Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

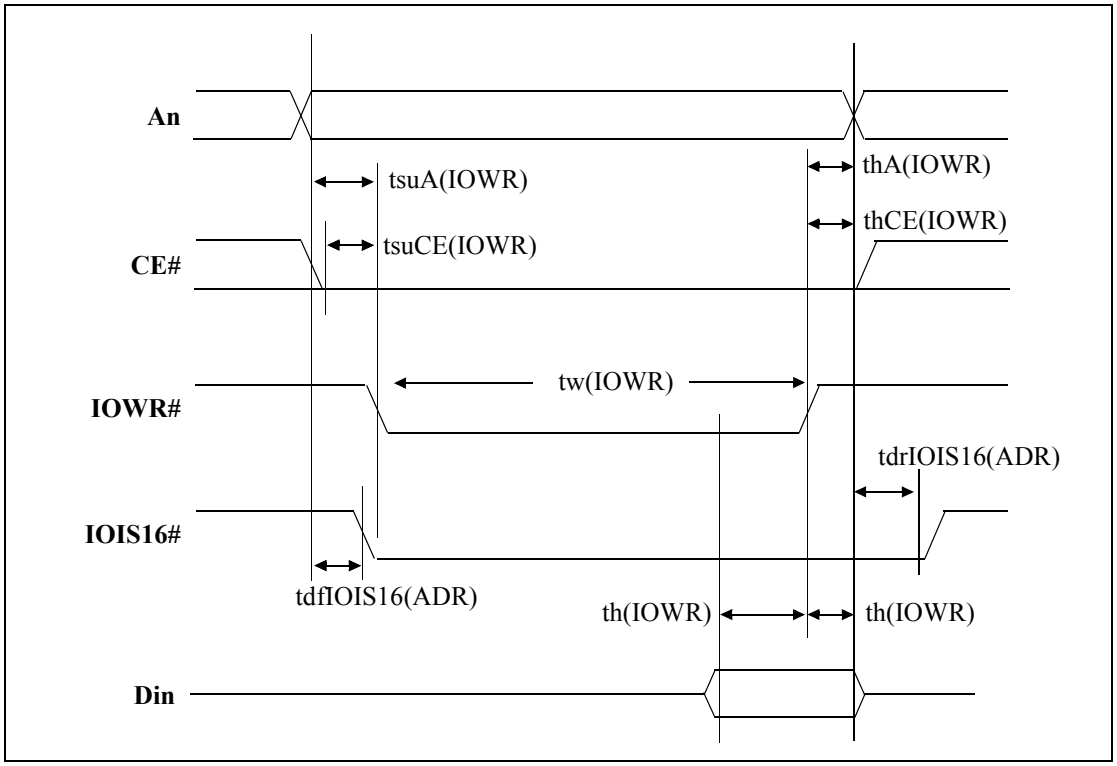
6.0.1 True IDE Mode Read Timing Diagram



6.0.2 True IDE Mode Write Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH		100
Data Hold following IOWR	th(IOWR)	tIWHDX	0	
IOWR Width Time	twl(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Assertion from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Negation from Address	tdrIOIS16(ADR)	tAVISH		35

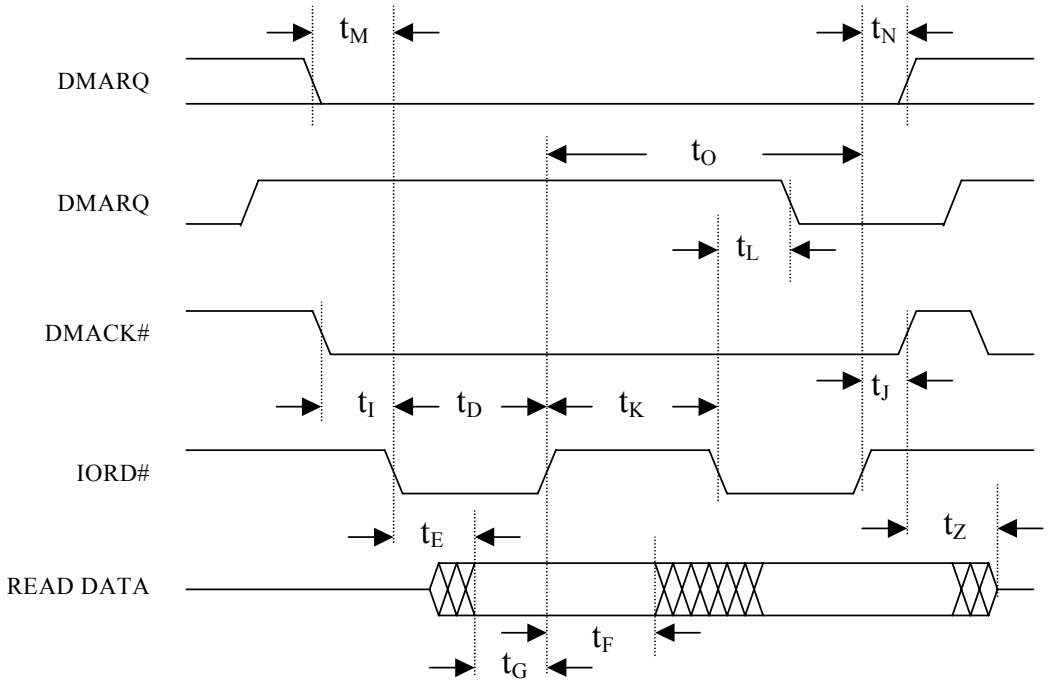
6.0.2 True IDE Mode Write Timing Diagram



6.0.3 True IDE DMA Mode Timing

Item	Symbol	Min. (ns)	Max. (ns)
Cycle Time	T_O		120
IORD asserted width	T_D	70	
IORD Data Access	T_E		50
IORD Data Hold	T_F	5	
IORD/IOWR Data Setup	T_G	20	
IOWR Data Hold	T_H	10	
DMACK to IORD/IOWR setup	T_I	0	
IORD/IOWR to DMACK hold	T_J	5	
IORD negated width	T_{KR}	25	
IOWR negated width	T_{KW}	25	
IORD to DMARQ delay	T_{LR}		35
IOWR to DMARQ delay	T_{LW}		35
CE valid to IORD/IOWR	T_M	25	
CE Hold	T_N	10	
DMACK	T_Z	25	

6.0.3 True IDE DMA Mode Read Timing Diagram



7.0 Electrical Characteristics

7.0.1 Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply Voltage	-0.3 ~7.0	V
V_{IN}	Input Voltage	-0.5 to $V_{DD + 0.3}$	V
I_{IN}	DC Input Current	-10	mA
T_{STG}	Storage Temperature	-65 to +150	^oC

7.0.2 Recommended Operating Conditions

Symbol	Parameter		Ratings	Unit
V_{DD}	Supply Voltage	5.0V	4.75 to 5.25	V
		3.3V	3.0 to 3.6	V
T_A	Operating Temperature	Commercial	0 to +70	^oC
		Industrial	-40 to +85	^oC

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7.0.3 DC Electrical Characteristics

(T_A = 0 to 70 ^oC V_{DD} = 3.3V +/- 0.3V)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input Voltage	CMOS		2.0		Vcc+0.3	V
V_{IL}	Low Level Input Voltage	CMOS		-0.5		0.8	V
V_T	Switching Threshold	CMOS			1.4		V
V_{T+}	Switching Threshold, Positive going threshold	CMOS				2.0	V
V_{T-}	Switching Threshold, Negative going threshold	CMOS		1.0			V
I_{IH}	High Level Input Current	Input Buffer	$V_{IN} = V_{DD}$	-10		10	uA
		Input Buffer with pull-up		10	30	60	uA
I_{IL}	Low Level Input Current	Input Buffer	$V_{IN} = V_{SS}$	-10		10	uA
		Input Buffer with pull-up		-160	-30	-10	uA
V_{OH}	High Level Output Current	Type 4(1)	I_{OH} = -4mA	2.4			V
		Type 8(2)	I_{OH} = -8mA				
		Type 16(3)	I_{OH} = -16mA				
V_{OL}	Low Level Output Current	Type 4(1)	I_{OH} = 4mA			0.4	V
		Type 8(2)	I_{OH} = 8mA				
		Type 16(3)	I_{OH} = 16mA				
I_{OZ}	Tri-state leakage current		$V_{OUT} = V_{SS}$ or V_{DD}	-10		10	uA
I_{DD}	Maximum Operating Current		V_{DD} = 3.3V f_{CLK} = 20MHz		30	40	mA
I_{idle}	Idle current					20	mA
I_{ds}	Stop current					30	uA

Notes:
1. 4mA drive output
2. 8mA drive output
3. 16mA drive output

7.0.3 DC Electrical Characteristics (contd.)
(T_A = 0 to 70 ^oC V_{DD} = 5V +/- 5%)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input Voltage	CMOS		3.5			V
		TTL		2.0			V
V_{IL}	Low Level Input Voltage	CMOS				1.5	V
		TTL				0.8	V
V_T	Switching Threshold	CMOS			2.5		V
		TTL			1.4		V
V_{T+}	Switching Threshold, Positive going threshold	CMOS				4.0	V
		TTL				2.0	V
V_{T-}	Switching Threshold, Negative going threshold	CMOS		1.0			V
		TTL		0.8			V
I_{IH}	High Level Input Current	Input Buffer	$V_{IN} = V_{DD}$	-10		10	uA
		Input Buffer with pull-up		10	50	100	uA
I_{IL}	Low Level Input Current	Input Buffer	$V_{IN} = V_{SS}$	-10		10	uA
		Input Buffer with pull-up		-100	-50	-10	uA
V_{OH}	High Level Output Current	Type 4(1)	I_{OH} = -4mA	2.4			V
		Type 8(2)	I_{OH} = -8mA				
		Type 16(3)	I_{OH} = -16mA				
V_{OL}	Low Level Output Current	Type 4(1)	I_{OH} = 4mA			0.4	V
		Type 8(2)	I_{OH} = 8mA				
		Type 16(3)	I_{OH} = 16mA				
I_{OZ}	Tri-state leakage current		V_{OUT} = V_{SS} or V_{DD}	-10		10	uA
I_{DD}	Maximum Operating Current		V_{DD} = 3.3V f_{CLK} = 20MHz		60	70	mA
I_{idle}	Idle current					35	mA
I_{ds}	Stop current					60	uA

Notes: 1. 4mA drive output 2. 8mA drive output 3. 16mA drive output

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