Revision History.

Rev.	Date	Details
A	December 20, 2004	New release

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16MB to 8GB ATA Flash PC Cards

1.0 General Description

1.1 Overview

The ATA Flash card brings power of data portability to mobile computing. It provides low power, high capacity mass storage in a small form factor and acts like a hard drive, but has the speed and transportability of solid state devices.

These cards are rugged, reliable and PCMCIA Card Type I compatible. They are available in 16MB, 32MB, 64MB, 128MB, 256MB, 512MB, 1GB, 2GB, 4GB, and 8GB capacities that are removable like floppy drives, but operate faster than hard disks.

Since there are no moving parts ATA Flash cards provide reliable operation in conditions that can be normally hostile to hard disk drives.

These cards operate at both 3.3V and 5.0V. This lower operating voltage compared to that of the hard drives means significantly less operating current, with lower heat dissipation, while avoiding the high current requirements of hard drive start-ups. Consequently overall throughput and productivity is increased because battery life of the portable equipment is extended.

Our ATA Flash cards are designed with an integrated controller chip and special proprietary space-management architecture to maximize read/write operations. This eliminates the firmware delays associated with sector read and write functions found in first generation flash cards. These cards are available for various applications such as Digital Film in consumer and professional still cameras, MP3 audio players, Consumer devices supporting WinCE, PocketPC, and a variety of other embedded and industrial applications.

1.2 Features

- PC Card Standard Release 8 Compliant
- Capacity Range 16MB to 8GB
- CIS (Card Information Structure) programmed into 256 Bytes of Attribute Memory
- Low power Dissipation
  - High Performance Read Current: 75mA @ 5V, 45mA @ 3.3V
  - High Performance Write Current: 85mA @ 5V, 55mA @ 3.3V
  - Sleep Mode: 300uA
- Supports Both PC Card ATA and True IDE Interface Modes
- Industrial Temp Range -40º C to +85º C (optional)
- DMA MW2 (BN controller)

1.3 Ordering Information

SMART Part Number	Chip Density	Physical Capacity	Sector Card	Head	Cylinder	Sector Track	Formatted Capacity
SM9FLAPC16J8x	128Mb	16MB	31,232	4	244	32	15,876,096
SM9FLAPC32J6x	256Mb	32MB	62,464	4	488	32	31,819,776
SM9FLAPC64J5x	512Mb	64MB	125,952	4	984	32	64,262,144
SM9FLAPC128D1x	1Gb	128MB	251,904	8	984	32	128,557,056
SM9FLAPC256D2x	2Gb	256MB	503,808	16	984	32	257,400,832
SM9FLAPC512D2x	2Gb	512MB	1,001,952	16	994	63	512,180,224
SM9FLAPC1024D2x	2Gb	1GB	2,014,992	16	1999	63	1,030,848,512
DMA support							
SM9FLAPC256N2x	2Gb	256MB	503,808	16	984	32	257,400,832
SM9FLAPC512N4x	4Gb	512MB	1,001,952	16	994	63	512,180,224
SM9FLAPC1024N9x	8Gb	1GB	2,014,992	16	1999	63	1,030,848,512
SM9FLAPC2048N9x	8Gb	2GB	4,029,984	16	3999	63	2,062,516,224
SM9FLAPC4096N9x	8Gb	4GB	8,053,920	16	7990	63	4,115,001,344
SM9FLAPC8192N9x	8Gb	8GB	16,128,000	16	16000	63	8,233,807,872

X: Operating Temperature Range

Blank - Commercial 0º C to 70º C

I - Industrial -40º C to + 85º C (Ref. to section 7.1.2, on page 103)

Part Number Decoding

SM	9	FLA	PC	128	M	1	I
SMART Modular	Memory Cards	ATA Flash	Product Type	Card Density	ATA Ctlr	Device Density	Operating Temperature Range
				16: 16MB 32: 32MB 64: 64MB 128: 128MB 256: 256MB 512: 512MB 1024: 1024MB 2048: 2048MB 4096: 4096MB 8192: 8192MB	M: Storm BM J: Twister AJ D: Twister ALA N: Storm BN	8: 128Mb 6: 256Mb 5: 512Mb 1: 1Gb 2: 2Gb 4: 4Gb 9: 8Gb	Blank: Commercial 0-70ºC I: Industrial -40 - +85ºC

Product Type:

CF: CF-Card (Compact Flash)

PC: PC-Card (ATA Type II, PCMCIA Card)

1.4 Specification Overview

1.4.1 Transfer Rates.

• Write Data Transfer Rate (Host to Flash)	6MB/sec (Capacity 128MB+) 3.6MB/sec (Capacity 64MB) 1.2MB/sec (Capacity <64MB)
• Host Interface Transfer Rate	16MB/s (burst with PIO Mode 4)
• Start-up Time (Sleep to Read/Write)	<10mS

1.4.2 Reliability.

• MTBF	> 1,000,000 hours
• Data reliability	1 in 10^{14} bits, read
• Endurance	> 2,000,000 erase/program cycles

1.4.3 Power Requirements

• VCC	5.0V±10%	3.3V±5%
• Read	75mA(max)	45mA(max)
• Write	85mA(max)	55mA(max)

1.4.4 Environmental Characteristics

• Shock	50G max. @ 11mS
• Vibration	15G peak to peak
• Operating temperature	0ºC to 70ºC (Commercial) -40º C to +85º C (Industrial)
• Storage temperature	-65ºC to 150ºC
• Humidity	5% to 95%
• Altitude	up to 80,000 ft.

1.4.5 Physical Dimensions

• Length	1.433 in. (36.40 mm.)
• Width	1.685 in. (42.80 mm.)
• Thickness	0.130 in. (3.30 mm.)
• Weight	0.36 Oz. (10.2 gm)

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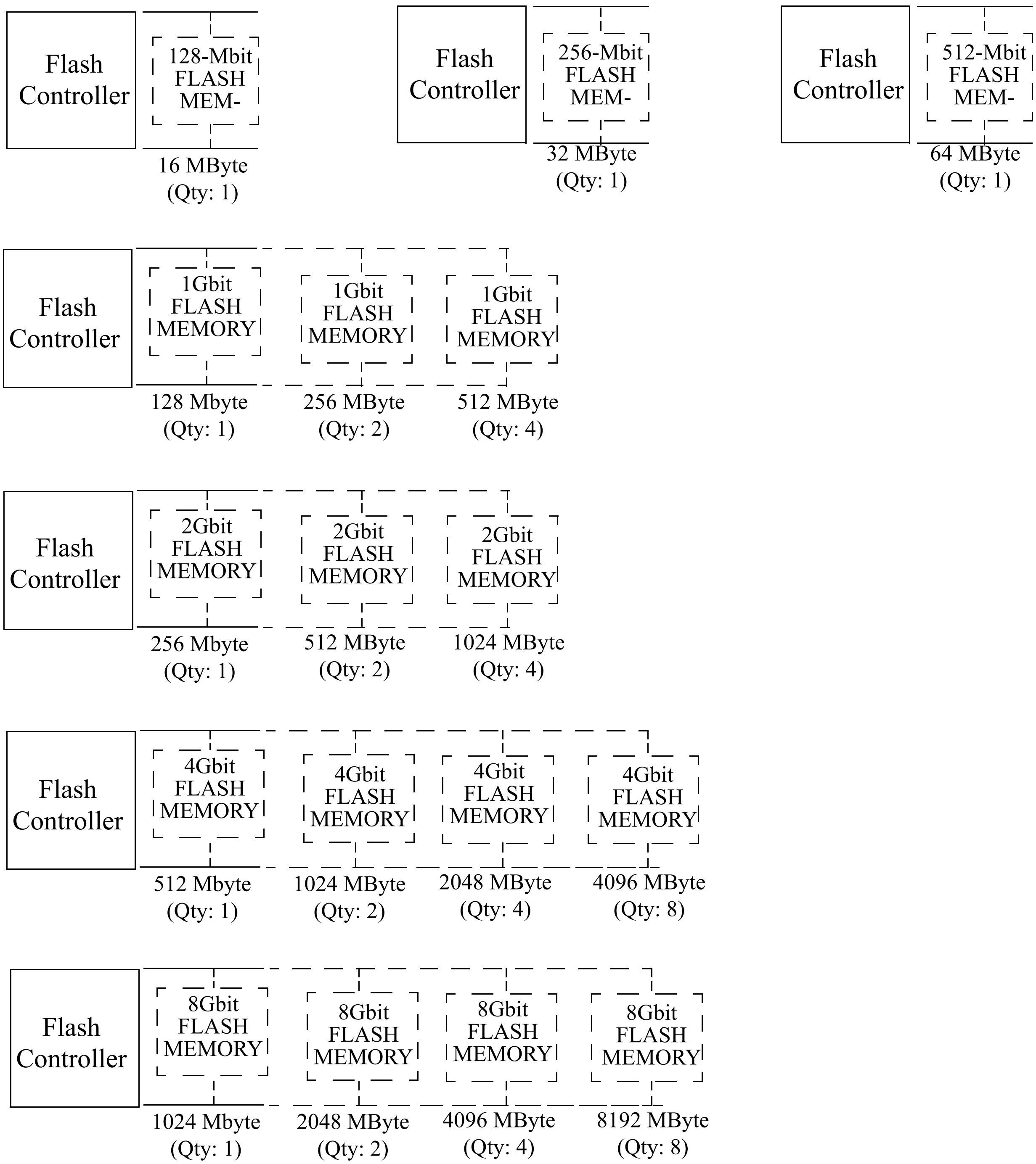
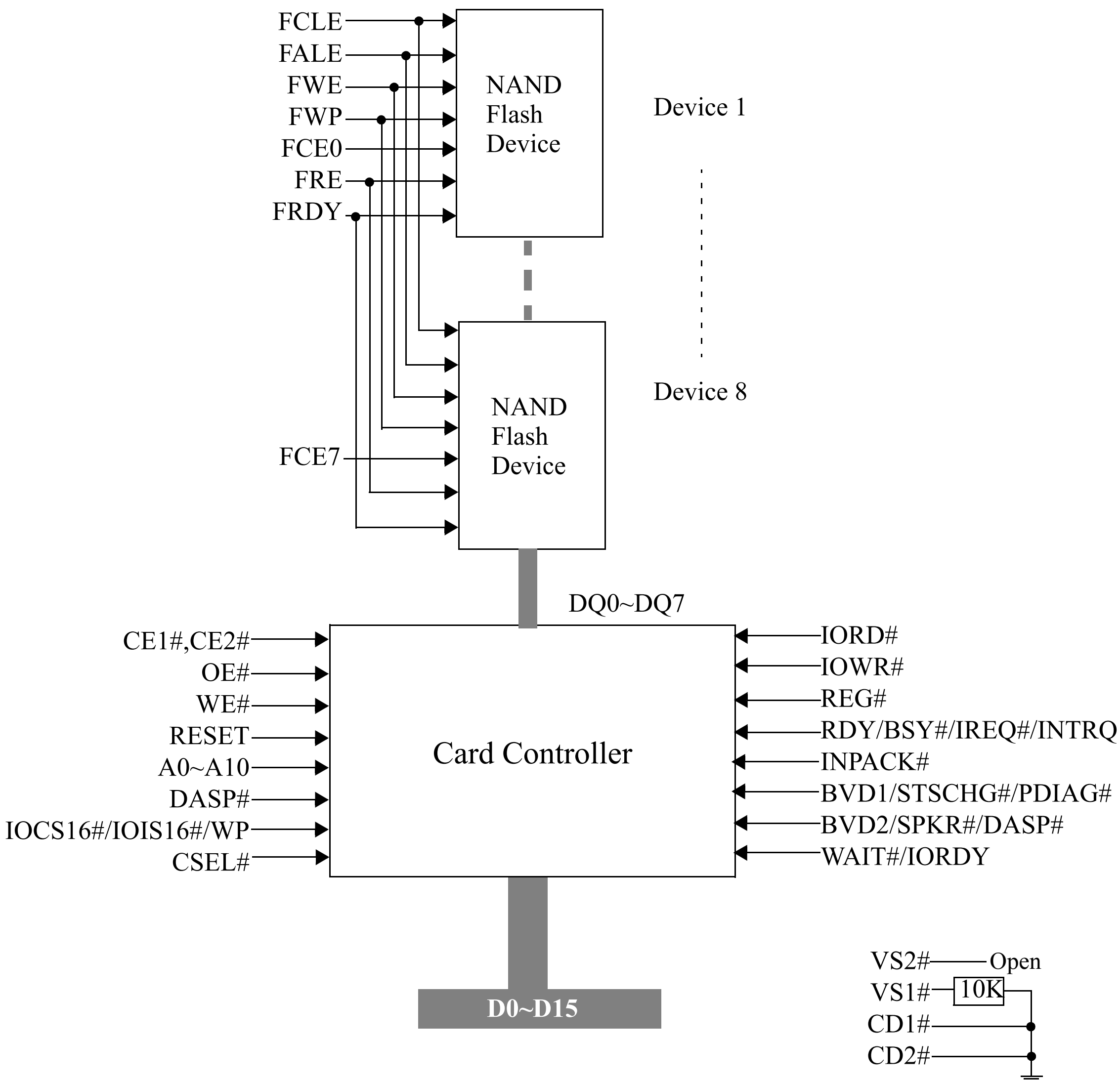
2.0 General Description

The ATA Flash Drive contains a ATA/IDE controller and flash memory devices in a Type I package with a 68-pin connector. The controller interfaces with the host system allowing data to be written to and read from the flash memory devices.



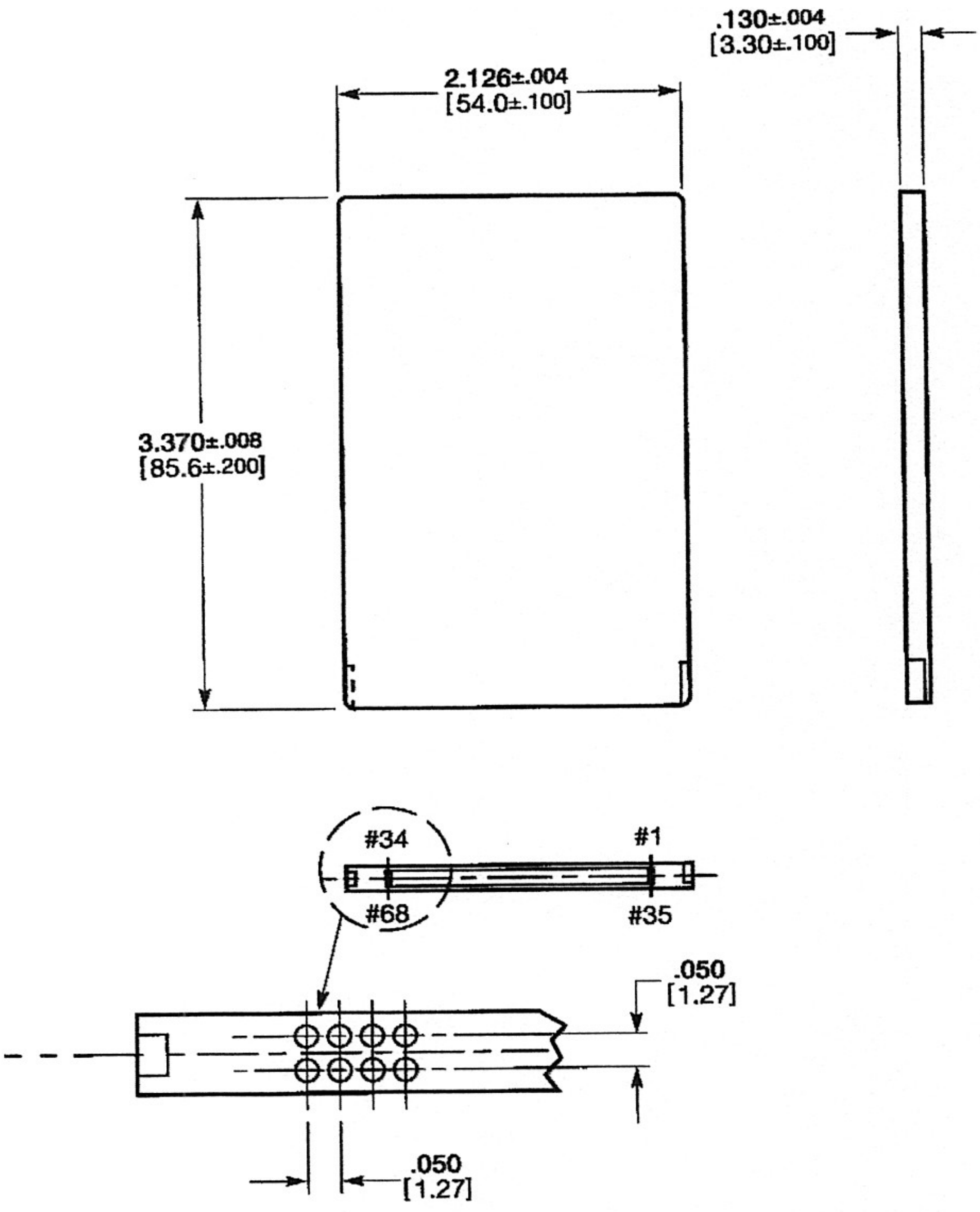
2.1 Functional Block Diagram



Notes :

1. All the signals shown going to the flash devices come from the card controller. All the other signals including those going to the card controller come from the Card Interface.

2.2 Mechanical Specifications for Type I ATA Flash PC Card



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3.0 Electrical Interface

3.1 Electrical Description

The Flash Cards are fully compliant with the ATA specification. This interface standard electrically complies with the PC Card ATA specifications, functioning in the I/O Mode, the Memory Mode, True IDE Mode.

Table 1 describes the I/O signals. Signals driven by the host are designated as inputs (I) while signals that are supplied by the ATA Flash Card are designated as are outputs (O). Bidirectional signals are designated as Input/Output (I/O). The ATA Flash Drive logic levels conform to those specified in the PCMCIA Release 2.1 specification. Table 2 describes the signals in the three different operating modes of the card. The three modes are Card Memory, Card I/O, and True IDE.

Table 1. Pin Assignments and Pin Type

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type
1	GND	Ground	1	GND	Ground	1	GND	Ground
2	D3	I/O	2	D3	I/O	2	D3	I/O
3	D4	I/O	3	D4	I/O	3	D4	I/O
4	D5	I/O	4	D5	I/O	4	D5	I/O
5	D6	I/O	5	D6	I/O	5	D6	I/O
6	D7	I/O	6	D7	I/O	6	D7	I/O
7	CE1#	I	7	CE1#	I	7	CS0#	I
8	A10	I	8	A10	I	8	A10[2]	I
9	OE#	I	9	OE#	I	9	OE#	I
10	NC	-	10	NC	-	10	NC	-
11	A9	I	11	A9	I	11	A9[2]	I
12	A8	I	12	A8	I	12	A8[2]	I
13	NC	-	13	NC	-	13	NC	-
14	NC	-	14	NC	-	14	NC	-
15	WE#	I	15	WE#	I	15	WE#[3]	I
16	RDY/BSY#	O	16	IREQ#	O	16	INTRQ	O
17	VCC	Power	17	VCC	Power	17	VCC	Power
18	NC	-	18	NC	-	18	NC	-
19	NC	-	19	NC	-	19	NC	-
20	NC	-	20	NC	-	20	NC	-
21	NC	-	21	NC	-	21	NC	-
22	A7	I	22	A7	I	22	A7[2]	I
23	A6	I	23	A6	I	23	A6[2]	I
24	A5	I	24	A5	I	24	A5[2]	I
25	A4	I	25	A4	I	25	A4[2]	I
26	A3	I	26	A3	I	26	A3[2]	I
27	A2	I	27	A2	I	27	A2	I
28	A1	I	28	A1	I	28	A1	I
29	A0	I	29	A0	I	29	A0	I
30	D0	I/O	30	D0	I/O	30	D0	I/O
31	D1	I/O	31	D1	I/O	31	D1	I/O
32	D2	I/O	32	D2	I/O	32	D2	I/O
33	WP	O	33	IOIS16#	O	33	IOCS16#	O
34	GND	Ground	34	GND	Ground	34	GND	Ground
35	GND	Ground	35	GND	Ground	35	GND	Ground

Table 1. Pin Assignments and Pin Type (Continued)

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	**Signal Name**	**Pin Type**	**Pin No.**	**Signal Name**	**Pin Type**	**Pin No.**	**Signal Name**	**Pin Type**
36	CD1#	O	36	CD1#	O	36	CD1#	O
37	D11[1]	I/O	37	D11[1]	I/O	37	D11[1]	I/O
38	D12[1]	I/O	38	D12[1]	I/O	38	D12[1]	I/O
39	D13[1]	I/O	39	D13[1]	I/O	39	D13[1]	I/O
40	D14[1]	I/O	40	D14[1]	I/O	40	D14[1]	I/O
41	D15[1]	I/O	41	D15[1]	I/O	41	D15[1]	I/O
42	CE2#[1]	I	42	CE2#[1]	I	42	CS1#[1]	I
43	VS1#	O	43	VS1#	O	43	VS1#	O
44	IORD#	I	44	IORD#	I	44	IORD	I
45	IOWR#	I	45	IOWR#	I	45	IOWR	I
46	NC	-	46	NC	-	46	NC	-
47	NC	-	47	NC	-	47	NC	-
48	NC	-	48	NC	-	48	NC	-
49	NC	-	49	NC	-	49	NC	-
50	NC	-	50	NC	-	50	NC	-
51	VCC	Power	51	VCC	Power	51	VCC	Power
52	NC	-	52	NC	-	52	VPP	-
53	NC	-	53	NC	-	53	NC	-
54	NC	-	54	NC	-	54	NC	-
55	NC	-	55	NC	-	55	NC	-
56	NC	-	56	NC	-	56	CSEL#	-
57	VS2#	O	57	VS2#	O	57	VS2#	O
58	RESET	I	58	RESET	I	58	RESET#	I
59	WAIT#	O	59	WAIT#	O	59	IORDY	O
60	INPACK#	O	60	INPACK#	O	60	DREQ	O
61	REG#	I	61	REG#	I	61	DMACK	I
62	BVD2	I/O	62	SPKR#	I/O	62	DASP#	I/O
63	BVD1	I/O	63	STSCHG#	I/O	63	PDIAG#	I/O
64	D8[1]	I/O	64	D8[1]		64	D8[1]	I/O
65	D9[1]	I/O	65	D9[1]	I/O	65	D9[1]	I/O
66	D10[1]	I/O	66	D10[1]	I/O	66	D10[1]	I/O
67	CD2#	O	67	CD2#	O	67	CD2#	O
68	GND	Ground	68	GND	Ground	68	GND	Ground

Note: 1. Signals marked with an asterick are required for 16-bit access, not required when installed in 8-bit systems.
2. Should be grounded by the host.

Table 2. Signal Description

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
CD1#, CD2#		O	36, 67	Card Detect Outputs
	PC Card Memory Mode			These Card Detect pins are connected to ground on the PC Card.They are used by the host to determine that the PC Card is fully inserted into the socket.
	PC Card I/O Mode			This signal is same in this mode.
	True IDE Mode			This signal is same in this mode.
IOWR#		I	45	I/O Write Input
	PC Card Memory Mode			This signal is not used in this mode.
	PC Card I/O Mode			The I/O Write strobe pulse is used to clock I/O data on the Card Data bus into the PC Card controller registers. The clocking will occur on the negative to positive going edge of the signal.
	True IDE Mode			This signal has the same function as in PC Card I/O Mode.
IORD#		I	44	I/O Read Input
	PC Card Memory Mode			This signal is not used in this mode.
	PC Card I/O Mode			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the PC Card.
	True IDE Mode			This signal has the same function as in PC Card I/O Mode.
WE#		I	15	Write Enable Input
	PC Card Memory Mode			This is a signal driven by the host and used for strobing memory write data to the registers of the PC Card. It is also used for writing the configuration registers.
	PC Card I/O Mode			In this mode, this signal is used to write the CIS and configuration registers.
	True IDE Mode			In this mode, this input signal is not used and should be connected to VCC by the host.

Table 2. Signal Description (continued)

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
OE#		I	9	Output Enable Input
	PC Card Memory Mode			This is a strobe generated by the host interface. It is used to read data from the PC Card and to read the CIS and configuration registers.
	PC Card I/O Mode			This signal is used to read the CIS and configuration registers.
	True IDE Mode			To enable the True IDE Mode, this input should be grounded by the host.
CE1#, CE2# / CS0#, CS1#		I	7, 42	Card Enable Inputs
CE1#, CE2#	PC Card Memory Mode			These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the odd byte of the word. CE1# accesses the even byte or the oddbyte of the word depending on A0 and CE2#. A multiplexing scheme based on A0, CE1#, CE2# allows 8 bit hosts to access all data on D0~D7.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
CS0#, CS1#	True IDE Mode			In the True IDE Mode, CS0# is the chip selectfor the task file registers while CS1# is used to select the Alternate Status Register and the Device Control Register.
WP / IOIS16# / IOCS16#		O	33	Write Protect / I/O Port 16 Output
WP	PC Card Memory Mode			The card does not have a WP switch. This signal is held low after reset initialization sequence.
IOIS16#	PC Card I/O Mode			A low signal indicated that a 16 bit or odd byte only operation can be performed.
IOCS16#	True IDE Mode			This signal is asserted low when the card is expecting a word data transfer cycle.
GND		Power	1, 34, 35, 68	Ground Pin
Vcc		Power	17, 51	Power Supply Pin (5.0V/3.3V)

Table 2. Signal Description (continued)

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
RESET/RESET#		I	58	Card Reset Input
RESET	PC Card Memory Mode			When this pin is high, this signal resets the Flash Card. The card Reset is only at power up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
RESET#	True IDE Mode			In this mode, this input pin is the active low from the host.
D15~D0		I/O	41, 40, 39, 38, 37, 66, 65, 64, 6, 5, 4, 3, 2, 32, 31, 30	16-bit Data Input/Output Bus
	PC Card Memory Mode			These lines carry the Data, Commands, and Status Information between the host and the controller. D15 is the MSB of odd byte and D7 the MSB of even byte in a Word Access.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
	True IDE Mode			All task file operations occur in byte mode on D7~D0, while all data transfers are word (16-bit) accesses.
A10~A0		I	8, 11, 12, 22, 23, 24, 25, 26, 27, 28, 29	Card Address Input Bus
	PC Card Memory Mode			These addresses along with the REG# signal are used to select the following: the I/O port address registers within the card, the memory mapped port address registers, a byte in the CIS and Configuration Control and Status registers.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
A2~A0	True IDE Mode	I	27, 28, 29	In this mode, only A2~A0 are used to select one of the eight Task File registers. All the remaining unused addresses should be grounded by the host.

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Table 2. Signal Description (continued)

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
REG#/DMACK#		I	61	Attribute Memory Select Input
REG#	PC Card Memory Mode			This signal is used to select between Register/ Attribute Memory (REG# = low) and Common Memory (REG# = high).
REG#	PC Card I/O Mode			Active Low on this signal will allow accesses to I/O space
DMACK#	True IDE Mode			This is a DMA Acknowledge signal that is asserted by the host in response to DREQ to initiate DMA transfers.
RDY/BSY# / IREQ# / INTRQ		O	16	Ready/Interrupt Request Output
RDY/BSY#	PC Card Memory Mode			This signal is set high when the card is ready to accept a new data transfer operation and held low when the card is busy. The host must have a pull-up resistor on this signal. When powering-up and when reset, the signal is held low (busy) until the card has completed the operation. When the signal indicates busy no operations to the card are permitted. This signal is held high whenever the card has been powered up with RESET# continuously disconnected or asserted.
IREQ#	PC Card I/O Mode			In this mode, this signal is used as for interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. This is set using Configuration Option Register.
INTRQ	True IDE Mode			In this mode, the signal is active high request to the host.
INPACK#/DREQ		O	60	Input Port Acknowledge Output
INPACK#	PC Card Memory Mode			This signal is not used in this mode.
INPACK#	PC Card I/O Mode			This signal is asserted by the card when the card is selected and is responding to an I/O read cycle. This signal is used by the host to enable the input data buffers between the host and the card.
DREQ	True IDE Mode			This signal is a DMA Request that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host

Table 2. Signal Description (continued)

Signal Name	Mode of operation	Pin Type	Pin No(s).	Description
CSEL#		I	56	Cable Select Input
	Card Memory Mode			This signal is not used in this mode.
	Card I/O Mode			This signal is not used in this mode.
	True IDE Mode			This signal is used to configure this device as Master or Slave. When this pin is grounded, this device is configured as Master. When this pin is tied to VCC this card is configured as Slave.
WAIT#/IORDY		O	59	Extend Bus Cycle/I/O Channel Ready Output
WAIT#	PC Card Memory Mode			This signal is driven low by the card to inform the host to delay completion of the cycle in progress.
	PC Card I/O Mode			This signal has the same function as in PC Card Memory Mode.
IORDY	True IDE Mode			This signal is negated to extend the host transfer cycle of any host register access (rear or write) when the card is not ready to respond to a data transfer request. When not negated, the signal is in high-impedance state.
BVD1/STSCHG#/ PDIAG#		O	63	Battery Voltage Detect Output / Card Status Changed Output / Passed Diagnostics Input/Output
BVD1	PC Card Memory Mode			This signal is asserted high since the card does not contain a battery.
STSCHG#	PC Card I/O Mode			This signal is asserted low to alert the host to changes in the RDY/BSY# and Write Protect states. Its use is controlled through the Card Configuration and Status Registers.
PDIAG#	True IDE Mode	I/O		This signal is asserted by slave drive to indicate to master drive that it has completed diagnostics and is ready to provide status.
BVD2 /SPKR# / DASP#		O	62	Battery Voltage Detect Output / Audio Waveform Output / Drive Active/Drive 1 Preset Output
BVD2	PC Card Memory Mode			This signal is asserted high since the card does not contain a battery.
SPKR#	PC Card I/O Mode			This signal is asserted high since the card does not support audio.
DASP#	True IDE Mode	I/O		This signal indicates that a drive is active or that a slave drive (Drive 1) is present.
VS1#, VS2#		O	43, 57	Voltage Sense Outputs
	All Modes			VS1# is grounded so that the Card's CIS can be read at 3.3V and VS2# is left open.

3.2 Card Configuration

3.2.1 Registers and Memory Space Decoding

CE2#	CE1#	REG#	OE#	WE#	A10	A9	A8~A4	A3	A2	A1	A0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Register Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit - D7~D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit - D15~D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bit - D15~D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Register Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit - D7~D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit - D15~D8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 bit - D15~D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (CIS Odd Byte Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (CIS Odd Byte Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (CIS Odd Byte Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (CIS Odd Byte Write)

3.2.2 Configuration Registers Decoding

CE2#	CE1#	REG#	OE#	WE#	A10	A9	A8~A4	A3	A2	A1	A0	Selected Space
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Register Read (200h)
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Register Write(200h)
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read (202h)
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write (202h)
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read (204h)
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write (204h)
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read (206h)
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write (206h)

Note: The location of the Card Configuration Registers should always be read from the CIS since these locations may vary in future products. No Writes should be performed to the Card Attribute Memory except to the Card Configuration Register Addresses. All other attribute memory locations are reserved.

3.3 Configuration Register Description

3.3.1 Configuration Option Register (Address 200h in attribute memory)

The Configuration Option Register is used to configure the card's interface, address decoding and interrupt and to issue a soft reset to the PC Card. This register is reset at System Power On and by the RESET signal (after the flash card is configured in PC Card or ATA extension mode).

Operation	B7	B6	B5	B4	B3	B2	B1	B0
R/W	SRESET	LevlREQ	CONF5	CONF4	CONF3	CONF2	CONF1	CONF0

SRESET — When this bit is set to logic one, the Host interface is in the reset state. This reset conditions is the same as a hardware or power-on reset state with the exception that this bit stays set, and the configuration as PCMCIA remains set. This software reset condition is removed when this bit is reset to logic zero. Following a power-on or hardware reset, this bit is cleared.

LevlREQ — This bit is set to one for level mode interrupt and set to zero for pulse mode interrupt. In pulse mode interrupt, the pulse width is at least 0.5uS. In level mode interrupt, the interrupt line is low state until the interrupt is serviced by the system. The interrupt is driven in the inactive state.

CONF5~CONF0 — Configuration Index. Set to zero by reset. It's used to select operation mode of the Card as shown below. Please note that CONF5 and CONF4 are reserved and must be written as zero. See the table below.

CONF5	CONF4	CONF3	CONF2	CONF1	CONF0	Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, 16 contiguous registers
0	0	0	0	1	0	Primary I/O Mapped, 1F0~1F7/3F6~3F7
0	0	0	0	1	1	Secondary I/O Mapped, 170~177/376~377

3.3.2 Card Status Register (Address 202h in attribute memory)

This register contains information about the card’s condition.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	Changed	SigChg	IOIs8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOIs8	0	0	PwrDwn	0	0

Changed — Indicates that one or both of the Pin Replacement Register CRdy, or CWProt bits are set to one.

SigChg — This field serves as a gate for the STSCHG# signal. When the card is configured as I/O interface, and if this and the Changed field are set to one, the function shall assert STSCHG#. If this field is reset to zero, the card shall not assert STSCHG#.

IOIs8 — The host sets this bit to a one if the Card is to be configured in an 8 bit I/O mode. The control for an 8-bit data access is built into the ATA command set, and still must be used.

PwrDwn — When the host sets this field to one, the card shall enter a power-down state. When this field is one, the host shall not access the card. The host shall return this field to zero before attempting to access the function. The host can set this function only if the card indicates it is ready. The RDY/BSY# value becomes busy when this bit is changed. RDY/BSY# will not become ready until the power state requested has been entered. The Card automatically powers down when it is idle and powers back up when it receives a command.

Int — This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the IEN# bit in the device control register, this bit is a zero.

3.3.3 Pin Replacement Register (Address 204h in attribute memory)

This register provides status for signals on the PC Card interface that are used in Memory Access Mode but assume a different meaning or use in I/O Mode. The register may be read and written; however, when written, the lower four bits act as a mask for changing the corresponding upper four bits.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	0	0	CRdy/Bsy#	CWProt	0	0	RRdy/Bsy	RWProt
Write	0	0	CRdy/Bsy#	CWProt	0	0	MRdy/Bsy	MWProt

CRdy/Bsy#	This bit is set to one when the bit RRdy/Bsy# changes state. This bit must be cleared by the host.
CWprot	This bit is set to one when the RWprot changes state.This bit must be cleared by the host.
RRdy/Bsy#	When read this bit represents the internal state of the RDY/BSY# signal. This bit may be used to read the state of RDY/BSY# as that pin has been reallocated to use as Interrupt Request when the card is configured as I/O interface.
RWprot	This bit is always zero, since the card does not support a WP switch.
MRdy/Bsy#	This bit acts as a mask for writing the corresponding CRdy/Bsy# bit.
MWprot	This bit acts as a mask for writing the corresponding CWprot bit.

Initial value of “C” bit	Written by Host		Final value of “C” bit	Comment
	“C” Bit	“M” Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by host
X	1	1	1	Set by host

3.3.4 Socket and Copy Register (Address 206h in attribute memory)

This register contains additional configuration information. This register may be used by the host system to implement a substitute for the ATA Master/Slave functionality. This register is always written by the system before writing the card's Configuration Index register.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	Reserved	Copy Number			Socket Number			
Write	0	Copy Number			Socket Number			

Reserved	This bit is reserved for future standardization. This bit must be set to zero by the software when the register is written.
Copy Number	Drive's which indicate in their CIS that they support more than one copy of identically configured drive-cards, should have a copy number in this field. Only 0 or 1 is allowed
Socket Number	This field indicates to the Flash Drive that it is located in the nth socket. The first socket is numbered 0.

3.4 Truth Tables (Transfer function tables)

3.4.1 Attribute Memory Table

REG#	CE2#	CE1#	A9	A0	OE#	WE#	D15~D8	D7~D0	Function Mode
X	1	1	X	X	X	X	High Z	High Z	Standby
0	1	0	0	0	0	1	High Z	Data	Read CIS (8 bits)
0	1	0	0	0	1	0	XX	Data	Write CIS (8 bits)
0	1	0	1	0	0	1	High Z	Data	Read Configuration Registers (8 bits)
0	1	0	1	0	1	0	XX	Data	Write Configuration Registers (8 bits)
0	0	0	0	X	0	1	Invalid	Data	Read CIS (16 bits)
0	0	0	0	X	1	0	XX	Data	Write CIS (16 bits)
0	0	0	1	X	0	1	Invalid	Data	Read Configuration Registers (16 bits)
0	0	0	1	X	1	0	XX	Data	Write Configuration Registers (16 bits)

Note: The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations.

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3.4.2 Common Memory Table

The common memory accesses can be either 8 bit or 16 bit. The Card permits both 8 and 16 bit accesses to all of its common memory addresses.
The Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the WAIT# signal at the start of the cycle.

REG#	CE2#	CE1#	A0	OE#	WE#	D15~D8	D7~D0	Function Mode
X	1	1	X	X	X	High Z	High Z	Standby Mode
1	1	0	0	0	1	High Z	Even Byte	Byte Read (8 bits)
1	1	0	1	0	1	High Z	Odd Byte	
1	1	0	0	1	0	XX	Even Byte	Byte Write (8 bits)
1	1	0	1	1	0	XX	Odd Byte	
1	0	0	X	0	1	Odd Byte	Even Byte	Word Read (16 bits)
1	0	0	X	1	0	Odd Byte	Even Byte	Word Write (16 bits)
1	0	1	X	0	1	Odd Byte	High Z	Odd Byte Read (8 bits)
1	0	1	X	1	0	Odd Byte	XX	Odd Byte Write (8 bits)

3.4.3 I/O Interface Table

The I/O accesses can be either 8 bit or 16 bit. when a 16 bit port is addressed the signal IOIS16# is asserted by the PC card. Otherwise this signal is de-asserted. If on the other hand, when a 16-bit transfer is attempted and this signal is not asserted, the host must generate a pair of 8-bit references to access the even and odd bytes.
The Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the WAIT# signal at the start of the cycle.

REG#	CE2#	CE1#	A0	IORD#	IOWR#	D15~D8	D7~D0	Function Mode
X	1	1	X	X	X	High Z	High Z	Standby Mode
0	1	0	0	0	1	High Z	Even Byte	Byte Input Access (8 bits)
0	1	0	1	0	1	High Z	Odd Byte	
0	1	0	0	1	0	XX	Even Byte	Byte Output Access (8 bits)
0	1	0	1	1	0	XX	Odd Byte	
0	0	0	0	0	1	Odd Byte	Even Byte	Word Input Access (16 bits)
0	0	0	0	1	0	Odd Byte	Even Byte	Word Output Access (16 bits)
1	X	X	X	0	1	XX	XX	I/O Read Inhibit
1	X	X	X	1	0	High Z	High Z	I/O Write Inhibit
0	0	1	X	0	1	Odd Byte	High Z	Odd Byte Input only (8 bits)
0	0	1	X	1	0	Odd Byte	XX	Odd Byte Output only (8 bits)

3.4.4 True IDE Mode Table

The Card can be configured in a True IDE Mode of operation. The Card can be configured in this mode only when the OE# signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the Card protocol and configuration are disabled and only I/O operations to the task file and Data Registers are allowed. In this mode no memory or attribute registers are accessible to the host.

Removing ATA Flash Card and re-inserting the card while the host is powered-on will reconfigure the card into ATA mode from the original True IDE mode. To configure the card in the True IDE mode, the socket must be powered cycled with the Card inserted and the OE# asserted.

CE2#	CE1#	A2~A0	DMACK#	IORD#	IOWR#	D15~D8	D7~D0	Function Mode
0	0	X		X	X	High Z	High Z	Invalid
1	1	X	1	X	X	High Z	High Z	Standby Mode
1	0	1-7h	1	1	0	XX	Data In	Task File Write
1	0	1-7h	1	0	1	High Z	Data Out	Task File Read
1	0	0	1	1	0	Odd Byte in	Even Byte in	PIO Data Register Write
1	1	X	0	1	0	Odd Byte in	Even Byte in	DMA Data Register Write
1	0	0	1	0	1	Odd Byte out	Even Byte out	PIO Data Register Read
1	1	X	0	0	1	Odd Byte out	Even Byte out	DMA Data Register Read
0	1	6h		1	0	XX	Control In	Control Register Write
0	1	6h		0	1	High Z	Status Out	All Status Read

3.5 ATA Specific Register Mapping

The Card can be configured as a high performance I/O device through

a. Standard PC-AT disk I/O address spaces 1F0h~1F7h, 3F6h~3F7h (primary), 170h~177h, 376h~377h (secondary) with IRQ14 (or other available IRQ).
b. Any system decoded 16 byte I/O block using any available IRQ.
c. Memory Space.

The communication to or from the Card is done using the Task File registers which provide all the necessary registers for control and status information. The Card interface connects peripherals to the host using four register mapping methods.The following is a detailed description of these methods:

Standard Configurations				
Config Index	**I/O or memory**	**Address**	**Drive#**	**Description**
0 & 8	Memory	0~Fh, 400~7FFh	0	Memory Mapped
1 & 9	I/O	xx0~xxFh	0	I/O Mapped 16 contiguous registers
2 & Ah	I/O	1F0h~1F7h, 3F6h~3F7h	0	Primary I/O Mapped Drive 0
2 & Ah	I/O	1F0h~1F7h, 3F6h~3F7h	1	Primary I/O Mapped Drive 1
3 & Bh	I/O	170h~177h, 376h~377h	0	Secondary I/O Mapped Drive 0
3 & Bh	I/O	170h~177h, 376h~377h	1	Secondary I/O Mapped Drive 1

3.5.1 Memory Mapped Addressing

When the Card registers are accessed via memory references, the registers appear in the common memory space window: 0~2K bytes as follows:

REG#	A10	A9~A4	A3	A2	A1	A0	Offset	OE# = 0	WE# = 0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Duplicate Even RD Data	Duplicate Even WR Data	2
1	0	X	1	0	0	1	9	Duplicate Odd RD Data	Duplicate Odd WR Data	2
1	0	X	1	1	0	1	D	Duplicate Error	Duplicate Feature	2
1	0	X	1	1	1	0	E	Alternate Status	Device Control	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

Notes:

1. Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
2. Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Therefore, if the registers are byte accessed in the order 9 and then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.
3. Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1K byte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some Card adapters also have auto incrementing logic embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Date Register FIFO and does not allow random access to the data buffer within the PC Card.

3.5.2 Contiguous I/O Mapped addressing

When the system decodes a contiguous block of I/O registers to select the PC Card, the registers are accessed in the block of I/O space decoded by the system as follows:

REG#	A3	A2	A1	A0	Offset	IORD# = 0	IOWR# = 0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Duplicate Even RD Data	Duplicate Even WR Data	2
0	1	0	0	1	9	Duplicate Odd RD Data	Duplicate Odd WR Data	2
0	1	1	0	1	D	Duplicate Error	Duplicate Feature	2
0	1	1	1	0	E	Alternate Status	Device Control	
0	1	1	1	1	F	Drive Address	Reserved	

Notes:

1. Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
2. Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Therefore, if the registers are byte accessed in the order 9 and then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.
3. Address lines which are not indicated are ignored by the Card for accessing all the registers in this table.

3.5.3 I/O Primary and Secondary Addressing

REG#	A9~A4	A3	A2	A1	A0	IORD# = 0	IOWR# = 0	Notes
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)h	0	0	0	1	Error	Features	2
0	1F(17)h	0	0	1	0	Sector Count	Sector Count	
0	1F(17)h	0	0	1	1	Sector No.	Sector No.	
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)h	0	1	1	1	Status	Command	
0	3F(37)h	0	1	1	0	Alternate Status	Drive Control	
0	3F(37)h	0	1	1	1	Drive Address	Reserved	

Notes:
1. Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
2. A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
3. Address lines which are not indicated are ignored by the Card for accessing all the registers in this table.

3.5.4 True IDE Mode addressing

When the Card is configured in the True IDE mode, the I/O decoding is as follows:

CE2#	CE1#	A2	A1	A0	DMACK#	IORD# = 0	IOWR# = 0
1	0	0	0	0	1	PIO RD Data	PIO WR Data
1	1	X	X	X	0	DMA RD Data	DMA WR Data
1	0	0	0	1	1	Error	Features
1	0	0	1	0	1	Sector Count	Sector Count
1	0	0	1	1	1	Sector No.	Sector No.
1	0	1	0	0	1	Cylinder Low	Cylinder Low
1	0	1	0	1	1	Cylinder High	Cylinder High
1	0	1	1	0	1	Select Card/Head	Select Card/Head
1	0	1	1	1	1	Status	Command
0	1	1	1	0	1	Alternate Status	Drive Control
0	1	1	1	1	1	Drive Address	Reserved

3.6 ATA Registers (Task File Registers)

The following section describes the hardware registers used by the host software to issue commands to the PC Card. These registers are often collectively referred to as the "Task File" registers.

Note: In accordance with the Card specifications, each of the registers which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15~D8) when CE1# is high and CE2# is low unless IOIS16# is high (not asserted) and I/O cycle is being performed.

3.6.1 Data Register (Address - 1F0/170; offset - 0, 8, 9)

CE2#	CE1#	A0	REG#	Offset	Data Bus	Data Register (Memory and I/O Mode)
0	0	X	_[a]	0, 8, 9	D15~D0	Word Data Register
1	0	0	_[a]	0, 8	D7~D0	Even Data Register
1	0	1	_[a]	9	D7~D0	Odd Data Register
0	1	X	_[a]	8, 9	D15~D8	Odd Data Register
1	0	1	_[a]	1, D	D7~D0	Error/Feature Register
0	1	X	_[a]	1	D15~D8	Error/Feature Register
0	0	X	_[a]	D	D15~D8	Error/Feature Register
CE2#	**CE1#**	**A0**	**DMACK#**	**Offset**	**Data Bus**	**Data Register (True IDE Mode)**
1	0	0	1	0	D15~D0	PIO Word Data Register
1	1	X	0	X	D15~D0	DMA Word Data Register
1	0	0	1	0	D7~D0	PIO Byte Data Register

a. REG# is mode dependent. Signal shall be 0 for I/O mode and 1 for Memory mode.

The data register is a 16 bit register and it used to transfer data blocks between the Card data buffer and the host. This register overlaps the Error register.

The table above describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general Word and byte access modes and operations.

3.6.2 Error Register (Address - 1F1/171; offset - 1, Dh; Read Only)

This register contains additional information about the source of an error when as error is indicated in bit 0 of the Status Register. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15~D8 during a write operation to offset 0 with CE2# low and CE1# high.

Bit 7 (BBK)	This bit is set when a Bad Block is detected. This bit is set when Error on Drive 1 (True IDE).
Bit 6 (UNC)	This bit is set when an Uncorrectable Read Error is encountered.
Bit 5	This bit is set to 0.
Bit 4 (IDNF)	The requested sector ID is in error or cannot be found.
Bit 3	This bit is set to 0.
Bit 2 (ABRT)	This bit is set if the command has been aborted because card status: Not Ready, Write Fault, or when an invalid command has been issued.
Bit 1	This bit is set to 0.
Bit 0 (AMNF)	This bit is set in case of a general error.

3.6.3 Feature Register (Address - 1F1/171; offset - 1, Dh; Write Only)

This register provides information regarding features of the Card that the host can utilize. This register is also accessed on data bits D15~D8 during a write operation to offset 0 with CE2# low and CE1# high.

3.6.4 Sector Count Register (Address - 1F2/172; offset - 2)

This register contains the number of sector.s of data requested to be transferred on a read or write operation between the host and the PC Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command competition. If not successfully completed, the register contains the number of sectors that need to be transferred to complete the request.

3.6.5 Sector Number (LBA 7~0) Register (Address - 1F3/173; offset - 3)

This register contains starting sector number or bits 7~0 of the Logical Block Address (LBA) for any Card data access for the subsequent command.

3.6.6 Cylinder Low (LBA 15~8) Register (Address - 1F4/174; offset - 4)

This register contains the low order 8 bits of the starting cylinder address or bits15~8 of the Logical Block Address (LBA).

3.6.7 Cylinder High (LBA 23~16) Register (Address - 1F5/175; offset - 5)

This register contains the high order 8 bits of the starting cylinder address or bits 23~16 of the Logical Block Address (LBA).

3.6.8 Drive/Head (LBA 27~24) Register (Address - 1F6/176; offset - 6)

The Drive/Head register is used to select the drive and head. It is also used to select the LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
1	LBA	1	DRV	HS3	HS2	HS1	HS0

Bit 7	This bit is set to 1.
Bit 6 (LBA)	LBA is a flag to select either cylinder/head/sector (CHS) or LBA Mode. When this bit is zero, CHS mode is selected. When this bit is one, LBA mode is selected. In LBA Mode, the LBA is interpreted as follows: LBA7~LBA0: Sector Number Register D7~D0 LBA15~LBA8: Sector Number Register D7~D0 LBA23~LBA16: Sector Number Register D7~D0 LBA27~LBA24: Sector Number Register HS3~HS0
Bit 5	This bit is set to 1.
Bit 4 (DRV)	DRV is the drive number. When DRV is zero, drive/card 0 is selected. When DRV is one, drive/card 1 is selected. The Card is set to be card 0 or 1 using the copy field (Drive#) of the Card Socket & Copy configuration register.
Bit 3 (HS3)	When operating in the CHS mode, this is bit 3 of the head number. It is Bit 27 when in LBA mode.
Bit 2 (HS2)	When operating in the CHS mode, this is bit 2 of the head number. It is Bit 26 when in LBA mode.
Bit 1 (HS1)	When operating in the CHS mode, this is bit 1 of the head number. It is Bit 25 when in LBA mode.
Bit 0 (HS0)	When operating in the CHS mode, this is bit 0 of the head number. It is Bit 24 when in LBA mode.

3.6.9 Status & Alternate Status Register (Address - 1F7/177 & 3F6/376; offset - 7, Eh; Read only)

This register returns the Card status when read by the host. Reading the status register does clear a pending interrupt while reading the alternate status register does not. The status and alternate status registers are read only registers. When writing to the address of the status register command register is written. When writing to the address of the alternate status register, device control register is written. The status bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

Bit 7 (Busy)	When the busy bit is set, the controller is executing a command. Also, when this bit is set, the host may not read or write any other register except the Status, Alternate Status, Device Control, or Drive Address registers. This bit is set when RESET# is asserted. It is also set when an AT host sets Device Control Register, Bit 2 or when the Command registers is loaded by the host.
Bit 6 (RDY)	RDY indicated whether the device is capable of performing Card operations. This bit is cleared at power up and remains cleared until the Card is ready to accept a command.
Bit 5 (DWF)	This bit, if set, indicates a write fault has occurred.
Bit 4 (DSC)	This bit is set when the Card is ready. This bit is cleared at power up.
Bit 3 (DRQ)	The bit is set when the Card requires that information be transferred either to or from the host through the data register.
Bit 2 (CORR)	This bit is set when a correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation. This bit is cleared when the Command register is written.
Bit 1 (0)	This bit is always set to 0.
Bit 0 (ERR)	This bit is set when the previous command has ended in some type of error. The bits in the error register contain additional information describing the error. This bit is cleared when the Command register is written.

3.6.10 Command Register (Address - 1F7/177; offset - 7; Write only)

The Command register contains the command code being sent to the device. Command execution begins immediately after this register is written.The Command register is a write only register. When reading from the address of the Command register, the Status register is read.

3.6.11 Device Control Register (Address - 3F6/376; offset - Eh; Write only)

This register is used to control the Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the card is BUSY. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	HD3En	SW Rst	IEn#	DMAEN

Bit 7 ~ Bit 4	These bits are don’t care. But it is recommended that the user program these bits to zero.
HD3En	This bit is set to enable bit 3 of the address of the selected drive head giving a 4-bit addressable range corresponding to 1 to 16 heads.
Bit 2 (SW Rst)	This bit is set to one in order to force the Card to perform an AT Disk controller soft reset operation. This does not change the Card configuration registers as hardware reset does. The card remains in reset until this bit is reset to zero.
Bit 1 (IEn#)	The interrupt enable bit enables interrupts when the bit is zero. When this bit is set to one interrupts from the Card are disabled. This bit also controls the Int bit in the configuration and status register. This bit is set to one at power on and reset.
DMAEN	The DMA Enable bit is an extra feature that this card supports for AT, that is not a generic AT interface. This feature allows a DMA channel to be multiplexed between multiple peripherals directly by the PC without local micro controller help. To enable this feature, the DMA mode must be selected in the Host Mode Control Register (Register 58H, bit 3), and the enable DMA control must be sent in the Misc. Control/Status Register (Register 52H, bit 4). With these two control bits set, the Device Control register bit 0 controls the DMA Enable of the DMA channel.

3.6.12 Drive Address Register (Address - 3F7/377; offset - Fh; Read only)

This is a diagnostic loop back register that contains Write Gate, Head Select3/Reduced Write Current, Head Select 2, Head Select 1, Head Select 0, Drive Select Drive 1, and Drive Select Drive 0. These bits reflect the state of the signals on the control cable. The host may read this register at any time. When host reads this register, only bits 6:0 are driven, bit 7 is High Impedance. NOTE: The Drive Address Register, also referred to as the Digital Input Register, is no longer supported in the ATA specifications. However, for backward compatibility, the ATA Flash Cards still supports this register, and responds as described.

B7	B6	B5	B4	B3	B2	B1	B0
HiZ	Wgate	H3/RWC	H2	H1	H0	DS1	DS0

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4.0 ATA Command Description

This section documents the Host Interface Commands supported by the Flash Card Controller. Two standard classes of Interface specifications are currently implemented: the AT Attachment interface specifications, and the CFA CompactFlash Specifications. In additions, this card conforms with the PC Card specifications when operating in the PC Card Mode and the ATA specifications when operating in the true IDE mode.

Each command is discussed in terms of the contents of the Task File when the command is issued, the contents of the Task File when the host read the status after the command is completed, as well as the data that is transferred in response to the command issued.

4.1 ATA Command Set

The table below summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

ATA Specification type	Command	Code
O	Check Power Mode	E5h or 98h
M	Executive Drive Diagnostic	90h
V	Erase Sector(s)	C0h
M	Format Track	50h
O	Identify Drive	ECh
O	Idle	E3h or 97h
O	Idle Immediate	E1h or 95h
M	Initialize Drive Parameters	91h
O	Read Buffer	E4h
O	Read DMA	C8h
M	Read Long Sector	22h or 23h
O	Read Multiple	C4h
M	Read Sector(s)	21h or 21h
M	Read Verify Sector(s)	40h or 41h
M	Recalibrate	1Xh
V	Request Sense	03h
M	Seek	7Xh
O	Set Features	EFh
O	Set Multiple Mode	C6h
O	Set Sleep Mode	E6h or 99h
O	Stand By	E2h or 96h
O	Stand By Immediate	E0h or 94h
V	Translate Sector	87h
V	Wear Level	F5h
O	Write Buffer	E8h
O	Write DMA	CAh
M	Write Long Sector	32h or 33h
O	Write Multiple	C5h
V	Write Multiple w/o Erase	CDh
M	Write Sector(s)	30h or 31h
V	Write Sector(s) w/o Erase	38h
O	Write Verify	3Ch

Note:

1. Type Abbreviation:
   - M - Mandatory Command
   - O - Optional Command
   - V - Vendor Unique Command
2. These type abbreviations pertain to the ATA Specifications only. In the case of Compact-Flash-ATA specifications, all Host commands listed here are Mandatory.

4.2 ATA Command Set Definition

This section details the functionality of commands supported by the Flash Card. For each command, the Command Block register contents for the command invoked by the Host, and the Command Block registers updated by the Flash Card after command completion, are shown. Following is an example of the command description, showing the conventions used for each command description. Throughout this document, the terms 'Task File' and 'Command Block' are used interchangeably to refer to the ATA I/O registers

.

A detailed description of the execution of the command is provided. This is followed by two tables, the first showing the requirements of the Command Block registers at the time that the Host issues the command to the Flash card, and the second showing the contents of the Command Block after completion or termination on error of the command.

Command Block specified by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	Command Code							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	Set Features Code							

The preceding table represents the contents of the Command Block registers when the command is issued by the Host. Where applicable, the Host first writes the appropriate data into the Features, Sector Count, Sector Number, Cylinder Hi/Low, and Drive/Head registers, and lastly, writes the command code into the Command register. The act of writing to the command register causes the Flash card to execute the command based on the contents of the Command Block at that instance.

Note that bits 7 and 5 of the Drive/Head register are denoted as 'nu.' Although the Host is expected to always set these bits to 1 when the command is issued, the Flash card ignores the value of these bits.

Command Block specified by Flash card upon completion/termination of 'Sample' command								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	V	0	V	0	V	0	0

The above table represents the contents of the Command Block registers upon completion of the command by the Flash card.

At the completion of every command, specific bits in the Status register is as follows: the BuSY, DriveWriteFault, DataReQuest, and InDeX bits are always de-asserted, while the DriveReaDY, and DriveSeekComplete bits are always asserted. The CORRected ECC bit and the ERRor bit are set or cleared as appropriate.

The contents of the Error register are always set to zero when a command is received, and are only valid if the ERR bit in the Status register is set to '1' at the completion of a command. In addition, the MediaChange, MediaChangeRequest, TracK0NotFound, and AddressMarkNotFound bits are always cleared, regardless of the state of the ERR bit in the Status register.

For the Command Block tables, explanations for each possible code are shown below:

L (LBA Mode bit)	This bit is used to specify whether the requested sector is addressed in the LBA mode or in the Cylinder-Head-Sector, CHS, mode. When set, the LBA mode is specified. The LBA is comprised of the lower significant nibble in the Drive/Head register, LBA[27:24], concatenated with the contents of the Cylinder Hi/Lo, and the Sector registers, LBA[23:0], respectively. If L=0, the sector is addressed in the classic Cylinder/Head/Sector CHS mode.
D (Drive Select bit)	This bit is used to select card 0 or 1, allowing up to two cards to share a single Task File. If two PC Card ATA cards are present in the system, one of the cards may be assigned as copy 0, and the second card may be assigned as copy 1, using the Copy field of the PCMCIA Socket & Copy card configuration register. In this case, the card designated as Copy 0 is selected when D=0. Conversely, the card designated as Copy 1 is selected when D=1.
1 (Bit is Set)	When referring to the Command Block registers when the Host issues a command, this bit must be set to a 1 by the Host before command invocation. When referring to the Command Block contents read by the Host after completion of a command, this bit is set by the Flash card upon command completion.
0 (Bit is Cleared)	When referring to the Command Block registers when the Host issues a command, this bit must be cleared to 0 by the Host before command invocation. When referring to the Command Block contents read by the Host after completion of a command, this bit is cleared by the Flash card upon command completion.
nu (Not Used)	Although the Host may specify this register/bit when invoking the command, the value for this command block register or bit is ignored by the card.
V (Valid Data)	When referring to the Command Block contents read by the Host after completion of a command, the value for the applicable bit is specified by the card.
na (Not Affected)	The value for this bit, or register, is neither set nor cleared by the card; i.e., it is unchanged by the card after command completion.

4.2.1 Check Power Mode

Although this command is supported for backward compatibility, it has no actual function. The card always returns the In Idle mode code ‘FFh’ in the Sector Count register, in response to this command. Command completion status always indicates command completed with no error.

Check Power Mode Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	98h/E5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Check Power Mode command (98h/E5h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	Power Mode Code is always FFh							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.2 Erase Sectors

This command erases the number of sectors specified in the Sector Count register, starting at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File.

Erase Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C0h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to eraser							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to eraser							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to erase							
SECTOR COUNT	The number of sectors/logical blocks to erase							
FEATURES	nu							

4.2.2 Erase Sectors (contd)

Command Block specified by Flash upon completion/termination of Erase Sectors command (C0h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	V	1	0	0	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector erased			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector erased							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector erased							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector erased							
SECTOR COUNT	The number of sectors that were not erased if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

4.2.3 Execute Drive Diagnostics

This command performs self-diagnostics on various internal components of the Flash card. Results of the test are reported in the Error register. Note that the bit definitions for the Error register do not apply in this command; rather, the value in the Error register is a diagnostic code, defined in the Table below.

Execute Drive Diagnostics Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	90h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Execute Drive Diagnostics command (90h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	Diagnostic Code. See Table below							

4.2.4 Format Track

Execute Drive Diagnostic Return Codes	
Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC logic error
05h	Controller microprocessor error
8xh	Slave Error[a]

a. Valid only if Flash card is in True IDE Mode.

This command erases 32 sectors starting at the sector specified by the Cylinder, Head, and Sector Number parameters in the task file. If the sector is not valid, an IDNF (ID Not Found) bit is set in the Error register and the command terminates.

In CHS mode, the number of sectors to format per track is set to the number of Current Sectors per Track in the Identify Drive data, by default 20h. Otherwise, it is set to the number of sectors per track as set by the Initialize Drive Parameters command.

In LBA mode, the number of sectors to format per track is specified by the Host in the Sector Count register. For backward compatibility, the Flash card accepts one sector of data from the Host. This data is not used.

Format Track Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	50h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	[LBA mode only] LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	[LBA mode only] The number of sectors to be formatted on the track.							
FEATURES	nu							

4.2.5 Identify Drive

Command Block specified by Flash card upon completion/termination of Format Track command (50h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

This command passes to the Host one sector of data describing the Flash card's parameters. See Table for a detailed description of the Identify Drive data.

Identify Drive Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Identify Drive command (ECh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

Drive Information		
Word	Data	Description
0	848Ah	General configuration bit-significant information:
1	Note 1	Number of Cylinders
2	0000h	Reserved
3	Note 1	Number of Heads
4	4000h	Number of unformatted bytes per track
5	0200h	Number of unformatted bytes per sector
6	Note 1	Number of sectors per track
7-9	0000h 0000h 0000h	Vendor unique
10-19	XXXXh	20 ASCII char serial number. Words 10-19 are filled with 20 ASCII ‘space’ chars.
20	0002h	Buffer type: Dual ported, multi-sector, w/read cache
21	0002h	Buffer size, in 512 byte increments
22	0004h	ECC length

Drive Information (Contd)

Word	Data	Description
23-26	V1.xx	Firmware revision, 8 ASCII chars where xx is minor revision number
27-46	[Manufacturer's info]	Model number, 40 ASCII chars.
47	0004h	Maximum Block Count=1 for Read/write Multiple commands
48	0000h	Cannot perform double word I/O
49	0200h	Capabilities: LBA supported, (0300h for DMA support)
50	0000h	Reserved
51	0200h	PIO timing mode 2,
52	0000h	Obsolete
53	0003h	Words 54 - 58 are valid
54	Note 1	Number of Current Cylinders
55	Note 1	Number of Current Heads
56	Note 1	Number of Current Sectors Per Track
57	Note 1	LSW of the Current Capacity in Sectors
58	Note 1	MSW of the Current Capacity in Sectors
59	0001h	Current Setting for Block Count=1 for R/W Multiple commands
60-61	Note 1	LSW of the total number of user addressable LBA's
62	0000h	Reserved
63	0X0Xh	Multiword DMA transfer. (0402h = MW2)
64	0003h	Advanced PIO modes supported
65	XXXXh	Minimum Multiword DMA transfer cycle time per word
66	XXXXh	Recommended Multiword DMA transfer cycle time
67	0078h	Minimum PIO transfer cycle time without flow control
68	0078h	Minimum PIO transfer cycle time with IORDY flow control
69-81	0000h	Reserved
82-84	0000h	Features/command sets supported

85-87	0000h	Features/command sets enabled
88	0000h	Reserved
89	0000h	Time required for Security erase unit completion
90	0000h	Time required for Enhanced Security erase unit completion
91	0000h	Current Advanced power management value
92-127	0000h	Reserved
128	0000h	Security status
129-159	0000h	Vendor unique bytes
160	0000h	Power requirement description
161	0000h	Reserved for assignment by the CFA
162	0000h	Key management schemes supported
163-175	0000h	Reserved for assignment by the CFA
176-255	0000h	Reserved

Note 1: This value is dependent upon the total capacity of the specific flash card.

4.2.6 Idle

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Idle Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	97h/E3h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Time-out Parameter. This parameter is ignored by the card.							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Idle command (97h/ E3h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.7 Idle Immediate

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Idle Immediate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	95h/E1h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Idle Immediate command (95h/E1h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.8 Initialize Drive Parameter

This command allows the Host to alter the number of sectors per track and the number of heads per cylinder. This enables Translation Mode which maps the flash storage using the altered parameters. On Host Reset, the default is 32 Sectors per Track and 8 Heads per Cylinder. The current values used for mapping are returned in the Identify Drive command as Number of Current Sectors per Track, and Number of Current Heads.

Initialize Drive Parameters Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	91h							
DRIVE/HEAD	nu	nu	nu	D	Number of Heads per Cyl minus 1			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	The Number of Sectors per Track							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Initialize Drive Parameters command (91h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.9 Read Buffer

This command transfers the current contents of the first page of the data buffer (512 bytes) to the Host.

Read Buffer Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	E4h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Read Buffer command (E4h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.10 Read DMA

This command transfers data from the Flash card to the Host using DMA. The data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register.

Read DMA Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	1	LBA	1	Drive	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

4.2.11 Read Long

This command is similar to the Read Sectors command except the contents of the Sector Count register are ignored and only one sector is read. The 512 data bytes and 4 ECC bytes are read into the buffer (with no ECC correction) and then transferred to the Host.

Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	22h (retries enabled) -or- 23h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the sector/ LBA to trans fer			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer. This should be set to 01 for compatibility							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Read Long command (22h/23h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] of the sector requested			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector requested							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector requested							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the sector requested							
SECTOR COUNT	00 if the command proceeded without error. 01 if an error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

4.2.12 Read Multiple

The R/W Multiple commands have to be enabled by a previous valid Set Multiple command. Once enabled, the Read Multiple command is identical to Read Sectors operation, except that the number of sectors as specified in the most recent Set Multiple command are transferred as a block to the Host without intervening Host handshaking. This number of sectors to transfer as a block is referred to as the block count. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block count is one. If Read Multiple has not been enabled, the ABRT (Aborted Command) bit is set in the Error register and the command terminates.

Read Multiple Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
	C4h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Read Multiple command (C4h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred. Zero otherwise.							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

4.2.13 Read Sectors

This command transfers data from the Flash card to the Host. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register.

Read Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	20h (retries enabled) -or- 21h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Read Sectors command (20h/21h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

4.2.14 Read Verify Sectors

The Read Verify Sectors command verifies one or more sectors on the card by transferring data from the Flash media to the data buffer in the card and verifying that the ECC is correct. It is performed identically to the Read Sectors command, except that DRQ is not asserted, and no data is transferred to the Host. If an uncorrectable error occurs, the read verify is terminated at the failing sector. The Command Block registers contain the CHS, or LBA of the sector in which the error occurred.

Read Verify Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	40h (retries enabled) -or- 41h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to verify							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to verify							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to verify							
SECTOR COUNT	The number of sectors/logical blocks to verify							
FEATURES	nu							

4.2.14 Read Verify Sectors (contd)

Command Block specified by Flash card upon completion/termination of Read Verify Sectors command (40h/41h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	na	H[3:0] or LBA[27:24] last sector verified, or sector where an unrecoverable error occurred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector verified, or sector where an unrecoverable error occurred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the sector verified, or sector where an unrecoverable error occurred							
SECTOR NUM	Sector or LBA[7:0] of the sector verified, or sector where an unrecoverable error occurred							
SECTOR COUNT	The number of sectors that were not yet verified if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	V	0	V	0	0	0	0

4.2.15 Recalibrate

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Recalibrate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	1xh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Recalibrate command (1xh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.16 Request Sense

This command returns an extended error code for the previous command which ended with an error. Table below defines and describes the contents of the Error register on completion of the Request Sense command.

Request Sense Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	03h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Request Sense command 03h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	See Table below							

Extended Error Codes	
Extended Error Code	Description
00h	No error detected
01h	Self test OK (no error)
09h	Miscellaneous error
20h	Invalid command
21h	Invalid address (Requested Head or Sector invalid)
2Fh	Address overflow (Address too large)
35h, 36h	Supply or generated voltage out of tolerance
11h	Uncorrectable ECC error
18h	Corrected ECC error
05h, 30-34h, 37h, 3Eh	Self test or diagnostic failed
10h, 14h	ID not found
3Ah	Spare sectors exhausted
1Fh	Data transfer error/Aborted command
0Ch, 38h, 3Bh, 3Ch, 3Fh	Corrupted media format
03h	Write/Erase failed

4.2.17 Seek

This command is supported for backward compatibility. Although this command has no actual function, it does perform a range check of valid track, and posts an IDNF error if the Head or Cylinder specified are out of bounds.

Seek Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	7xh							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the track			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the track							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the track							
SECTOR NUM	(Valid in LBA mode only) LBA[7:0] of the track							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Seek command (7xh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	V	0	0	0	0

4.2.18 Set Features

This command allows the Host to control various card features. Each feature is selected by passing its feature code in the Features register. Certain features use additional information passed in the Sector Count register. If the Feature register contains a feature code that is not supported, the drive will respond by setting the Error bit in the Status register and the Abort bit in the Error register.

Set Features Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	EFh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR START	nu							
SECTOR COUNT	nu (additional info if features code is 97h or 9Ah)							
FEATURES	Feature Code. See Table on page […]							

Command Block specified by Flash card upon completion/termination of Set Features command (EFh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na (8: maximum current divided by 4 if feature code is 9Ah)							
CYLINDER LOW	na (2: minimum current divided by 4 if feature code is 9Ah)							
SECTOR	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

Valid Feature Codes	
Code	Feature
01h	Enable 8-bit data transfers
03h	Set transfer mode based on value in Sector Count register
44h	NOP; accepted for backward compatibility
55h	NOP; accepted for backward compatibility
66h	Disable restoration of default features with Soft Reset
69h	NOP; accepted for backward compatibility
81h	Disable 8-bit data transfer
96h	NOP; accepted for backward compatibility
97h	Control clock using value in Sector Count register
9Ah	Control current using value in Sector Count register
Aah	NOP; accepted for backward compatibility
BBh	NOP; accepted for backward compatibility
CCh	Enable restoration of default features with Soft Reset

NOTES

Feature codes 01h and 81h controls Host transfer data width. By default, 8-bit transfers are disabled.

Feature codes 44h, 55h, 69h, 96h, AAh, and BBh are supported for backward compatibility and have no function.

Feature codes 66h and CCh control whether or not a Soft Reset restores any feature codes to their Power On default value. The features effected are 81h (8-bit transfer), 97h (clock control), and 9A (current control). By default, a Soft Reset will restore the default features.

Feature code 03h allows the host to select the PIO or Multiword DMA transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode shall be selected at all times. For Cards which support DMA, one Multiword DMA mode shall be selected at all times. The host may change the selected modes by the Set Features command.

Trasfer Mode Values		
Bits (7:3)	Bits (2:0)	Mode
00000b	000b	PIO default mode
00000b	001b	PIO default mode, disable IORDY
00001b	Mode	PIO flow control transfer mode
00100b	Mode	Multiword DMA mode

Feature code 9Ah enables the card to self-configure to best meet the Host system's power requirements. The Host sets a value in the Sector Count register that is equal to one-fourth of the desired maximum average current (in mA) that the card should consume. For example, if the Sector Count register is set to 6, the card will self-configure to provide the best possible performance without exceeding 24 mA. Upon completion of the command, the card responds to the Host with the range of values supported by the card. The minimum value is set in the Cylinder Low register, and the maximum value is set in the Cylinder Hi register. The card will accept values outside this programmable range, but will operate either at the lowest power or highest performance as appropriate.

4.2.19 Set Multiple

This command is used either to set the block count (number of sectors per block), simultaneously enabling R/W Multiple command support, or to disable support of R/W Multiple commands. Although setting, reading, and writing blocks are supported, the only valid block count is one. If the block count specified by the Host is greater than one, the command is aborted. The ERR bit in the Status register is set, and the ABRT bit in the Error register is set. In addition, Read Multiple and Write Multiple commands are disabled. If the contents of the Sector Count register is '1', Read Multiple and Write Multiple commands are enabled until the next Host RESET. Invoking this command with Sector Count = 0 disables R/W Multiple commands. In this case, all subsequent R/W Multiple commands issued by the Host are aborted by the Flash card.

Set Multiple Command Issued by Host

Task File Register	7	6	5	4	3	2	1	0
COMMAND	C6h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	01: R/W Multiple command transfer enabled, 00: R/W Multiple command transfer disabled							
FEATURES	nu							

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4.2.19 Set Multiple (contd)

Command Block specified by Flash card upon completion/termination of Set Multiple command (C6h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	V	0	0

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4.2.20 Sleep

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Sleep Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	99h/E6h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Sleep command (99h/E6h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

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4.2.21 Standby

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Standby Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	96h/E2h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	Time-out Parameter. This is ignored by the Flash card							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Standby command (96h/E2h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.22 Standby Immediate

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Standby Immediate Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	94H/E0h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Standby Immediate command (94H/E0h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.23 Translate Sector

This command transfers one block of data to the Host relating to the sector specified in the Task File. See Table below for a detailed description of this data.

Translate Sector Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	87h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the sector/LBA							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Translate Sector command (87h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

Translate Sector Data Description	
Byte Address	Description
00h	00h
01h	Cylinder LSB
02h	Head
03h	Sector
04h-06h	LBA
07h-12h	00h
13h	Erased flag
14h-17h	00h
18h-1Ah	Hot Count (not supported)
1Bh-1FFh	00h

4.2.24 Wear Leveling

Although this command is supported for backward compatibility, it has no actual function. The card always returns good status at the completion of this command.

Wear Leveling Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	F5h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Wear Leveling command (F5h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	0	0	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	00							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.25 Write Buffer

This command transfers 512 bytes of data from the Host to the first page of the data buffer.

Write Buffer Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	E8h							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Write Buffer command (E8h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	0
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	0	0	0	0	0	0	0	0

4.2.26 Write DMA

This command transfers data from the Host to the Flash card. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register. If the address of the starting sector is not within the range of addresses supported by this card, the IDNF (ID Not Found)) bit is set in the Error register and the command terminates.

Write Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	CAh							
DRIVE/HEAD	1	LBA	1	Drive	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

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4.2.27 Write Long

This command is similar to the Write Sectors command except the contents of the Sector Count register are ignored and only one sector is written. The 512 data bytes and 4 ECC bytes are transferred from the Host and then written from the buffer to the flash.

Write Long Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	32h (retries enabled) -or- 33h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer. Should be set to 1 for compatibility.							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Write Long command (32h/33h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	1 if an unrecoverable error occurred, 0 if the command proceeded successfully							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	V0

4.2.28 Write Multiple

The R/W Multiple commands have to be enabled by a previous valid Set Multiple command. Once enabled, the Write Multiple command is identical to Write Sectors operation, except that the number of sectors as specified in the most recent Set Multiple command are transferred as a block from the Host without intervening Host handshaking. This number of sectors to transfer as a block is referred to as the block count. Although the Set Multiple, and R/W Multiple commands are supported, the only valid block count is one. If Write Multiple has not been enabled, the ABRT (Command Aborted) bit is set in the Error register and the command terminates.

Write Multiple Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C5h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Write Multiple command (C5h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

4.2.29 Write Multiple Without Erase

This command is supported for backward compatibility. The actual function performed is identical to the Write Multiple command.

Write Multiple without Erase Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	CDh							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Write Multiple without Erase command (CDh)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

4.2.30 Write Sectors

This command transfers data from the Host to the Flash card. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers in the Task File, and proceeds for the number of sectors specified in the Sector Count register. If the address of the starting sector is not within the range of addresses supported by this card, the IDNF (ID Not Found)) bit is set in the Error register and the command terminates.

Write Sectors Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	30h (retries enabled) -or- 31h (retries disabled)							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Write Sectors command (30h/31h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

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4.2.31 Write Sectors Without Erase

This command is supported for backward compatibility. The actual function performed is identical to the Write Sectors (with retry) command.

Write Sectors w/o Erase Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	C8h							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Write Sectors w/o Erase command (C8h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

4.2.32 Write Verify

This command is similar to the write sectors (without retry) command except that each sector is verified after being written.

Write Verify Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	3Ch							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Write Verify command (3Ch)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	L	na	na	H[3:0] or LBA[27:24] last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TK0NF	AMNF
	V	0	0	V	0	0	0	0

5.1 Card Information Structure

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
00h	01h	CISTPL_DEVICE								Device Info Tuple	Tuple Code
02h	03h	CISTPL_LINK								Link is 3 bytes	Link to next Tuple
04h	D9h	Device Type Code Dh = I/O				W 1	Device Speed 1			I/O device, No WP Speed=250ns	Device ID WPS, Device Speed
06h	03h	Device Size								32K of Address Space	Device size
08h	FFh	List End Marker								End of Devices	End Marker
0Ah	1Ch	CISTPL_DEVICE_OC								Device other con- dition Tuple	Tuple Code
0Ch	04h	CISTPL_LINK								Link is 4 bytes	Link to next Tuple
0Eh	03h	Reserved					vcc 01		M wait 1	3.3Vcc Operation	Vcc, PCMCIA 2.0 Timing
10h	D9h	Device Type Code Dh= I/O				WPS 1	Device Speed 1				Device ID WPS, Device Speed
12h	01h	Device Size								2k Byte Address Space	Device Size
14h	FFh	List End Marker								End of Devices	End of Marker
16h	18h	CISTPL_JEDEC_C								JEDEC ID Common Memory	Tuple Code
18h	02h	CISTPL_LINK								Link is 2 bytes	Link to next Tuple
1Ah	DFh	PCMCIA Manufacturer's ID									Byte 1, JEDEC ID of Device 1
1Ch	01h	PCMCIA Code for PC card ATA No Vpp Required								Second Byte of JEDEC ID	Byte 2 JEDEC ID
1Eh	20h	CISTPL_MANFID								Manufacturer ID	Tuple Code
20h	04h	CISTPL_LINK								Link is 4 bytes	Link to next Tuple
22h	01h	Card Manufacturer's Code								Smart JEDEC Manufacturer's ID	TPLMID_MANF

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5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
24h	32h										TPLMID_MANF
26h	00h	Manufacturer's Information									TPLMID_MANF
28h	00h										TPLMID_MANF
2Ah	15h	CISTPL_VERS_1								Level 1 version	Tuple Code
2Ch	2Bh	CISTPL_LINK								Link is 29 bytes	Link to next Tuple
2Eh	04h	TPPLV_MAJOR								PCMCIA 2.0/ JEIDA 4.1	Major Version
30h	01h	TPPLV_MINOR								PCMCIA 2.0/ JEIDA 4.1	Minor Version
32h	53h	ASCII Manufacturing String								S	Info String 1
34h	4Dh									M	
36h	41h									A	
38h	52h									R	
3Ah	54h									T	
3Ch	20h									Space	
3Eh	41h									A	
40h	54h									T	
42h	41h									A	
44h	20h									Space	
46h	46h									F	
48h	6Ch									l	
4Ah	61h									a	

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
4Ch	73h									s	
4Eh	68h									h	
50h	20h									Space	
52h	43h									C	
54h	61h									a	
56h	72h									r	
58h	64h									d	
5Ah	20h									Space	
5Ch	20h									Space	
5Eh	20h									Space	
60h	20h									Space	
62h	20h									Space	
64h	00h	End of Manufacturing								Null Terminator	
66h	54h	ASCII Product String								T	Info String 2
68h	49h									I	
6Ah	44h									D	
6Ch	41h									A	
6Eh	4Ch									L	
70h	57h									W	
72h	56h									V	
74h	00h									Null Terminator	
76h	53h	Additional Information								S	
78h	48h									H	
7Ah	30h									0	

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
7Ch	30h									0	
7Eh	32h									2	
80h	00h	End of CIS Revision Number								Null Terminator	
82h	FFh	List End Marker									End of Marker
84h	21h	CISTPL_FUNCID								Control ID Tuple	Tuple Code
86h	02h	CISTPL-LINK								Link is 2 bytes	Link to next Tuple
88h	04h	IC Card Function Code								FIXED DISK Fuction	TPLFID_FUNCTION
8Ah	01h	R 0	R 0	R 0	R 0	R 0	R 0	R 0	P 1	Attempt installa-tion at Post P: Install at POST R: Reserved	
8Ch	22h	CISTPL_FUNCE								Function Exten-sion Tuple	Tuple Code
8Eh	02h	CISTPL_LINK								Link is 2 bytes	Link to next Tuple
90h	01h	Disk Function Extension Tuple Type								Disk Device inter-face	TPLFE_TYPE
92h	01h	Interface Type Code								PC Card-ATA interface	TPLFE_DATA
94h	22h	CISTPL_FUNCE								Function Exten-sion Tuple	Tuple Code
96h	03h	CISTPL_LINK								Link is 3 bytes	Link to next tuple
98h	02h	Disk Function Extension Tuple Type								PCMCIA-ATA Extension Tuple	Extension Tuple Type for Disk
9Ah	04h	R 0	R 0	R 0	R 0	U 0	S 1	V 0		Silicon Drive V:0 No Vpp required S: Silicon U: ID Drive not Mfg/SN unique R: Reserved	TPLFE_DATA

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
9Ch	5Fh	R 0	I 1	E 0	N 1	P3 1	P2 1	P1 1	P0 1	Sleep, Stand by, Idle Mode Supported. P0: Sleep Mode supported P1: Stanby Mode supported P2: Idle Mode supported P3: Drive Auto Power Control not supported N: Same Primary or Secondary I/O addressing exclude 3F7H E: Index bit Not Emulated I: IOIS16 is asserted on twin configuration R: Reserved	
9Eh	1Ah	CISTPL_CONFIG								Configuration Tuple	Tuple Code
A0h	05h	CISTPL_LINK								Link is 5 bytes	Link to next Tuple
A2h	01h	RFSZ 00		RMSZ 0000				RASZ 01		Size of Field RFSZ: reserved Field RMSZ: Reg Mask RASZ: Base Address	TPCC_SZ
A4h	03h	TPCC_LAST								Entry Index 03h	Last entry of Configuration table
A6h	00h	TPCC_RADR (LSB)								Configuration Registers are located at 200h	Location of Config Registers
A8h	02h	TPCC_RADR (MSB)									
AAh	0Fh	R 0	R 0	R 0	R 0	S 1	P 1	C 1	I 1	4 Configuration registers are present I: Configuration Index C: Configuration & Status P: Pin replacement S: Socket and Copy R: Reserved for future	TPCC_RMSK

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
ACh	1Bh	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
AEh	0Bh	CISTPL_LINK								Link is 11 bytes	Link to next Tuple
B0h	C0h	I 1	D 1	Configuration Index 000000						Memory Mapped I/O D: Default Configuration I: Interface Byte Follows	TPCE_INDEX
B2h	40h	W 0	R 1	P 0	B 0	Interface Type 0000				Interface: Memory only BVD & WP not used, RDY/BSY# & Wait# used for Memory Cycle B: Battery Volt detects P: Write Protect R: RDY/BSY# W: Wait used for Memory Cycle	TPCE_IF
B4h	A1h	M 1	MS 01		IR 0	IO 0	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info not present IO: I/O port info not present IR: Interrupt info not present MS: Mem space info type M: misc. info bytes present	TPCE_FS
B6h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV1	Nominal operating supply voltage. NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for Vcc
B8h	55h	X 0	Ah = 5.0				5h = 1V			Vcc Nominal is 5 Volts	Vcc Nominal Value
BAh	4Dh	X 0	9h = 4.5				5h = 1V			Min V Parameter is 4.5V	Vcc Min Value

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
BCh	5Dh	X 0	Bh = 5.5				5h = 1V			Max Parameter is 5.5V	Vcc Max Value
BEh	75h	X 0	Eh =8				5h = 10mA			Peak I Parameter is 8mA	I Max Value
C0h	08h	Length in 256 byte pages (LSB)								Length of Mem Space is 2KB	TPCE_MS Length LSB
C2h	00h	Length in 256 bytes pages (MSB)								Start at 0 on card	TPCE_MS Length MSB
C4h	21h	X 0	R 0	P 1	RO 0	A 0	Twin 1			Power Down T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc. Features	TPCE_MI
C6h	1Bh	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
C8h	06h	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
CAh	00 h									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
CCh	01h	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
CEh	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage. NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
D0h	B5h			Mantissa			Exponent			Nom Voltage =3.0V	Vcc nominal value
D2h	1Eh				Extension					+0.3V	Extension byte
D4h	4Dh			Mantissa			Exponent			Peak I Parameter 2.5mA	Max avg cur-rent
D6h	1Bh	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
D8h	0Dh	CISTPL_LINK								Link is 13 bytes	Link to next Tuple
DAh	C1h	I 1	D 1	Configuration Index 000001						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDEX
DCh	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF
DEh	99h	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info present IO: I/O port info present IR: Interrupt info present MS: No memory space M: Misc. info bytes present	TPCE_FS

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
E0h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal operating supply voltage. NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
E2h	55h	X 0	Ah = 5.0				5h = 1V			VCC Nominal is 5 Volts	VCC Nominal Value
E4h	4Dh	X 0	9h = 4.5				5h = 1V			Min V Parameter is 4.5V	Vcc Min Value
E6h	5Dh	X 0	Bh = 5.5				5h = 1V			Max Parameter is 5.5V	Vcc Max Value
E8h	75h	X 0	Eh =8				5h = 10mA			Peak I Parameter is 8mA	I Max Value
EAh	64h	R 0	S 1	E 1	IO Add Lines 00100					Supports both 8/16bit I/O accesses	TPCE_IO
ECh	F0h	S 1	P 1	L 1	M 1	V 0	B 0	I 0	N 0	IRQ Sharing Logic Active Pulse & Level mode interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Bit Mask of IRQ V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Mask able IRQ	TPCE_IR
EEh	FFh	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 1	IRQ Levels to be routed 0~7 recommended	TPCE_IR Mask Extension
F0h	FFh	F 1	E 1	D 1	C 1	B 1	A 1	9 1	8 1	IRQ Levels to be routed 8~15 recommended	TPCE_IR Mask Extension

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
F2h	21h	X 0	R 0	P 1	R O 0	A 0	Twin 001			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: More Misc. Fields Byte	TPCE_MI
F4h	1Bh	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
F6h	06h	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
F8h	01 h									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
FAh	01h	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
FCh	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage. NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
FEh	B5h	Mantissa				Exponent				Nom Voltage =3.0V	Vcc nominal value
100h	1Eh	Extension								+0.3V	Extension byte
102h	4Dh	Mantissa				Exponent				Peak I Parameter 2.5mA	Max avg current

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
104h	1Bh	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
106h	12h	CISTPL_LINK								Link is 18 bytes	Link to next tuple
108h	C2h	I 1	D 1	Configuration Index 000010						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDX
10Ah	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF
10Ch	99h	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info present IO: I/O port info present IR: Interrupt info not present MS: No Mem space M: misc. info bytes present	TPCE_FS
10Eh	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal operating supply voltage. NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for Vcc
110h	55h	X 0	Ah = 5.0				5h = 1V			VCC Nominal is 5 Volts	VCC Nominal Value
112h	4Dh	X 0	9h = 4.5				5h = 1V			Min V Parameter is 4.5V	
114h	5Dh	X 0	Bh = 5.5				5h = 1V			Max Parameter is 5.5V	
116h	75h	X 0	Eh =8				5h = 10mA			Peak I Parameter is 8mA	

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
118h	EAh	R 1	B 1 1				I/O 10h			I/O Space Addresses Bus 16/8: Register accessible by 8 or 16 bits I/O: A 1 kbyte I/O address space	TPCE_IO
11Ah	61h	L 01		A 10		I/O				L: Length 1 byte long A: Address is 4 bytes long	
11Ch	F0h									1st I/O base address (LSB)	1st I/O range address
11Eh	01h									1st I/O base address (MSB)	
120h	07h									1st I/O length - 1	1st I/O range length
122h	F6h									2nd I/O base address (LSB)	2nd I/O range address
124h	03h									2nd I/O base address (MSB)	
126h	01h									2nd I/O length - 1	2nd I/O range length
128h	EEh	S 1	P 1	L 1	M0	V 1	B 1	I 1	N 0	IRQ Sharing Logic Active Pulse & Level mode interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Not IRQ Mask Computer Mask 4000h V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Mask able IRQ	TPCE_IR

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
12Ah	21h	X 0	R 0	P 1	RO 0	A 0	Twin 001			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc. Features	TPCE_MI
12Ch	1Bh	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
12Eh	06h	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
130h	02h									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
132h	01h	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
134h	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage. NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
136h	B5h			Mantissa			Exponent			Nom Voltage =3.0V	Vcc nominal value
138h	1Eh				Extension					+0.3V	Extension byte
13Ah	4Dh			Mantissa			Exponent			Peak I Parameter 2.5mA	Max avg current
13Ch	1Bh	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
13Eh	12h	CISTPL_LINK								Link is 18 bytes	Link to next Tuple

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
140h	C3h	I 1	D 1	Configuration Index 000011						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDX
142h	41h	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF
144h	99h	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info present IO: I/O port info present IR: Interrupt info not present MS: No Mem space M: misc. info bytes present	TPCE_FS
146h	27h	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal operating supply voltage. NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for Vcc
148h	55h	X 0	Ah = 5.0				5h = 1V			Vcc Nominal is 5 Volts	Vcc Nominal Value
14Ah	4Dh	X 0	9h = 4.5				5h = 1V			Min V Parameter is 4.5V	Vcc Min Value
14Ch	5Dh	X 0	Bh = 5.5				5h = 1V			Max Parameter is 5.5V	Vcc Max Value
14Eh	75h	X 0	Eh =8				5h = 10mA			Peak I Parameter is 8mA	I Max Value
150h	EAh	R 1	B 11		I/O 10h					I/O Space Addresses Bus 16/8: Register accessible by 8 or 16 bits I/O: A 1 kbyte I/O address space	TPCE_IO

5.1 Card Information Structure (Contd.)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
152h	61h	L 01		A 10		I/O				L: Length 1 byte long A: Address is 4 bytes long	
154h	70h									1st I/O base address (LSB)	1st I/O range address
156h	01h									1st I/O base address (MSB)	
158h	07h									1st I/O length - 1	1st I/O range length
15Ah	76h									2nd I/O base address (LSB)	2nd I/O range address
15Ch	03h									2nd I/O base address (MSB)	
15Eh	01h									2nd I/O length - 1	2nd I/O range length
160h	EEh	S 1	P 1	L 1	M0	V 1	B 1	I 1	N 0	IRQ Sharing Logic Active Pulse & Level mode interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Not IRQ Mask Computer Mask 4000h V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Mask able IRQ	TPCE_IR
162h	21h	X 0	R 0	P 1	RO 0	A 0	Twin 001			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc. Features	TPCE_MI
164h	1Bh	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
166h	06h	CISTPL_LINK								Link is 6 bytes	Link to next Tuple

5.1 Card Information Structure (Contd.)

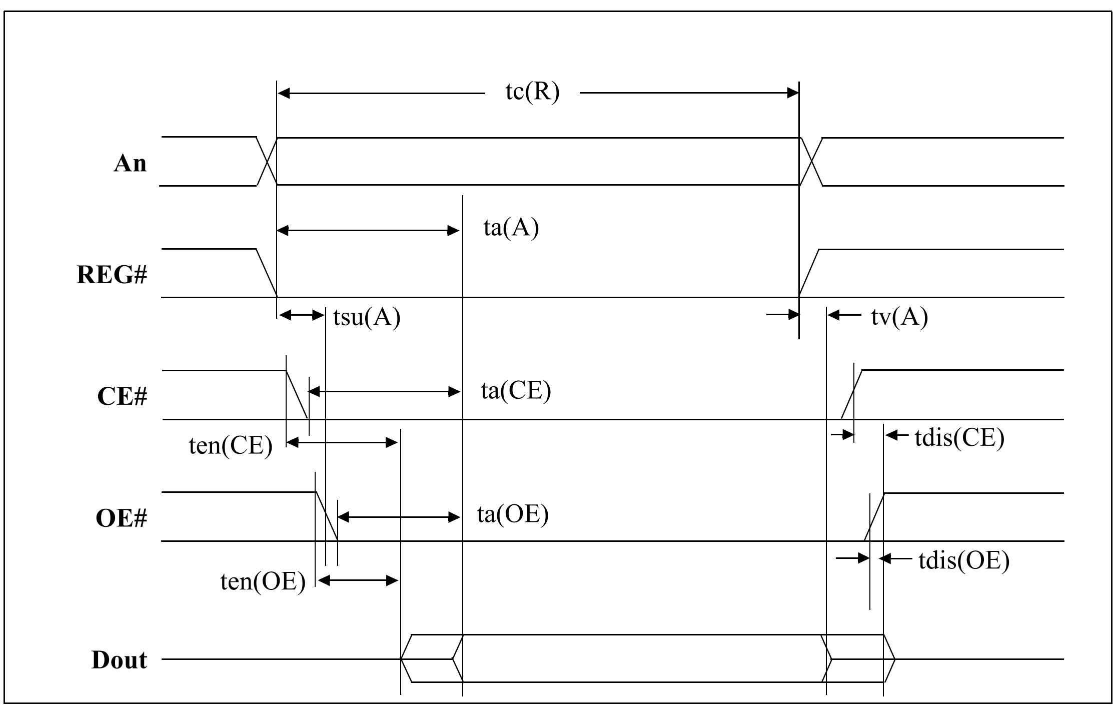
Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
168h	03h									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
16Ah	01h	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
16Ch	21h	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage. NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
16Eh	B5h	Mantissa Exponent								Nom Voltage =3.0V	Vcc nominal value
170h	1Eh	Extension								+0.3V	Extension byte
172h	4Dh	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
174h	14h	CISTPL_NO_LINK								No link Tuple	Tuple Code
176h	00h	No Bytes Following								Link is 0 bytes	Link to next Tuple
178h	FFh	CISTPL_END								End of list Tuple	Tuple Code

6.1 Timing Information

6.1.1 Attribute Memory Read Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVWL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXQX	0	

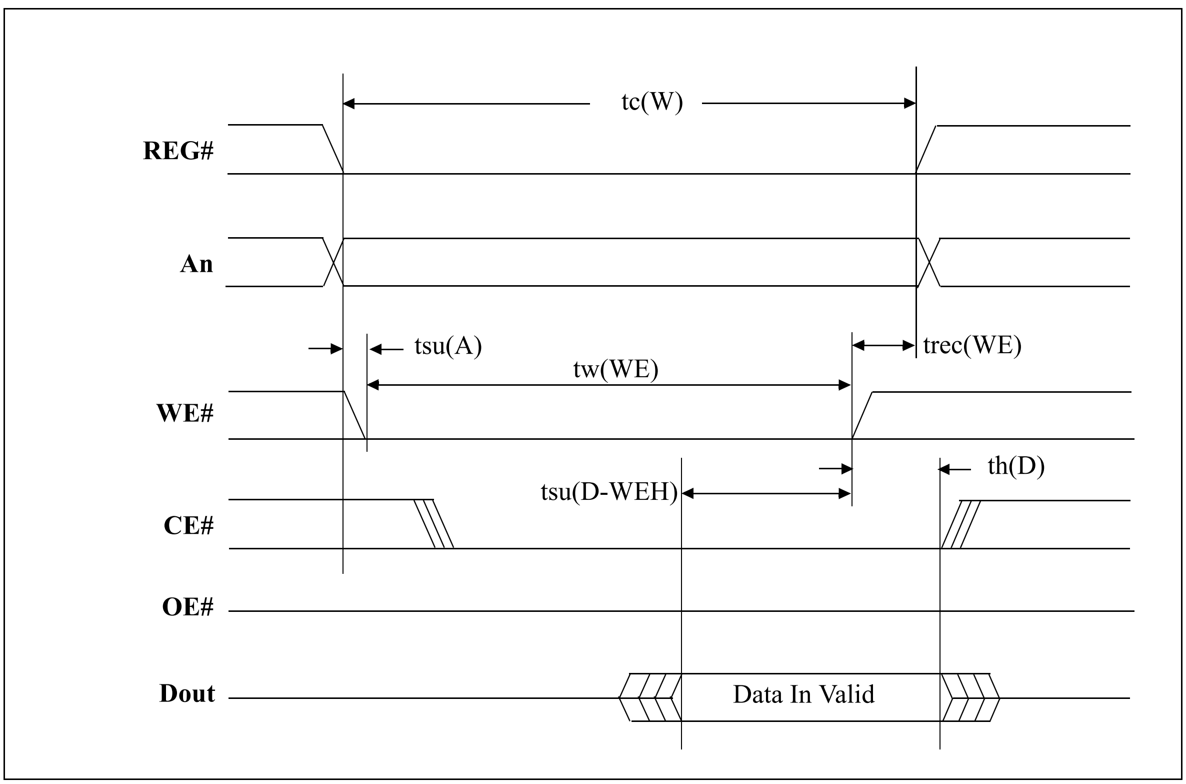
6.1.1 Attribute Memory Read Timing Diagram



6.1.2 Attribute Memory Write Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	

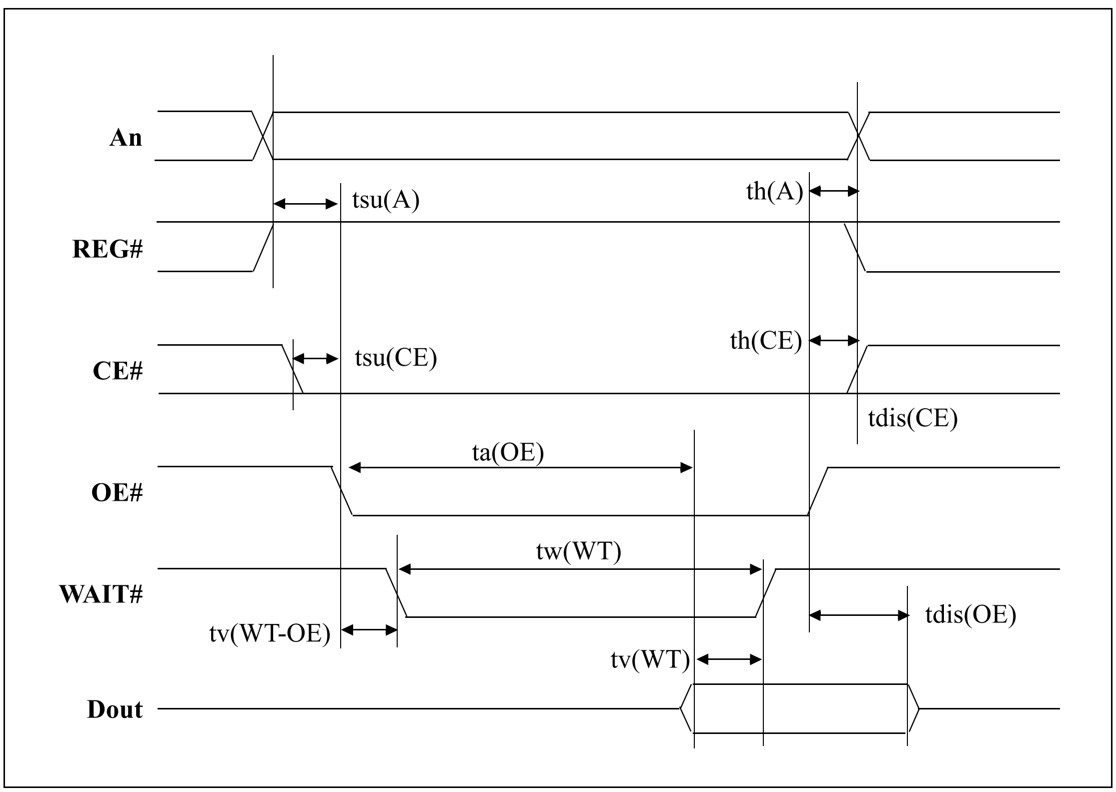
6.1.2 Attribute Memory Write Timing Diagram



6.1.3 Common Memory Read Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Output Enable Access Time	ta(OE)	tGLQV		125
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVGL	30	
Address Hold Time	th(A)	tGHAX	20	
CE Setup before OE	tsu(CE)	tELGL	0	
CE Hold following OE	th(CE)	tGHEH	20	
Wait Delay Falling from OE	tv(WT-OE)	tGLWTV		35
Data Setup for Wait Release	tv(WT)	tQVWTH		0
Wait Width Time	tw(WT)	tWTLWTH		350

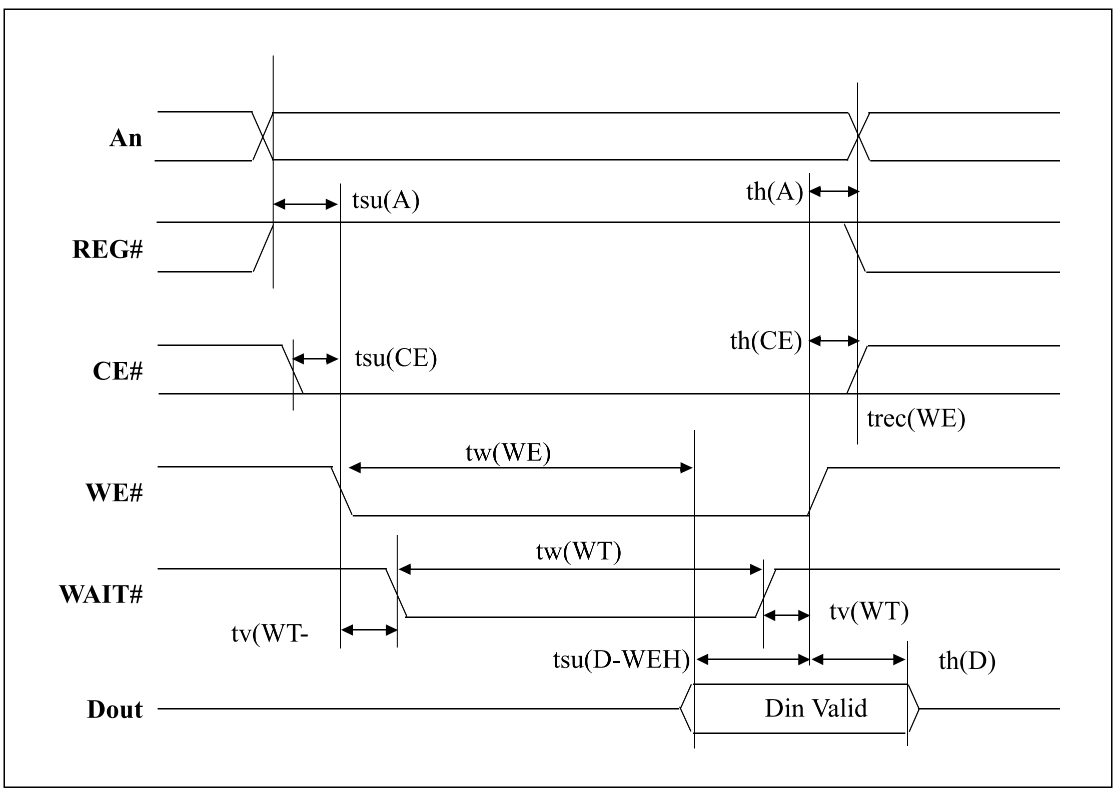
6.1.3 Common Memory Read Timing Diagram



6.1.4 Common Memory Write Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before WE	tsu(D-WEH)	tDVWH	80	
Data Hold following WE	th(D)	tIWMDX	30	
WE Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
CE Setup before WE	tsu(CE)	tELWL	0	
Write Recovery Time	trec(W)	tWMAX	30	
Address Hold Time	th(A)	tGHAX	20	
CE Hold following WE	th(CE)	tGHEH	20	
Wait Delay Failing from WE	tv(WT-WE)	tWLWTV		35
WE high from Wait Release	tv(WT)	tWTHWH	0	
Wait Width Time	tw(WT)	tWTLWTH		350

6.1.4 Common Memory Write Timing Diagram



6.1.5 I/O Memory Read Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
REG setup before IORD	tsuREG(IORD)	tRGLIGL	5	
REG Hold following IORD	thREG(IORD)	tIGHRGH	0	
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45
NPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IORD	tdWT(IORD)	tIGLWTL		35
Data Delay from Wait Release	td(WT)	tWTHQV		0
Wait Width Time	tw(WT)	tWTLWTH		350

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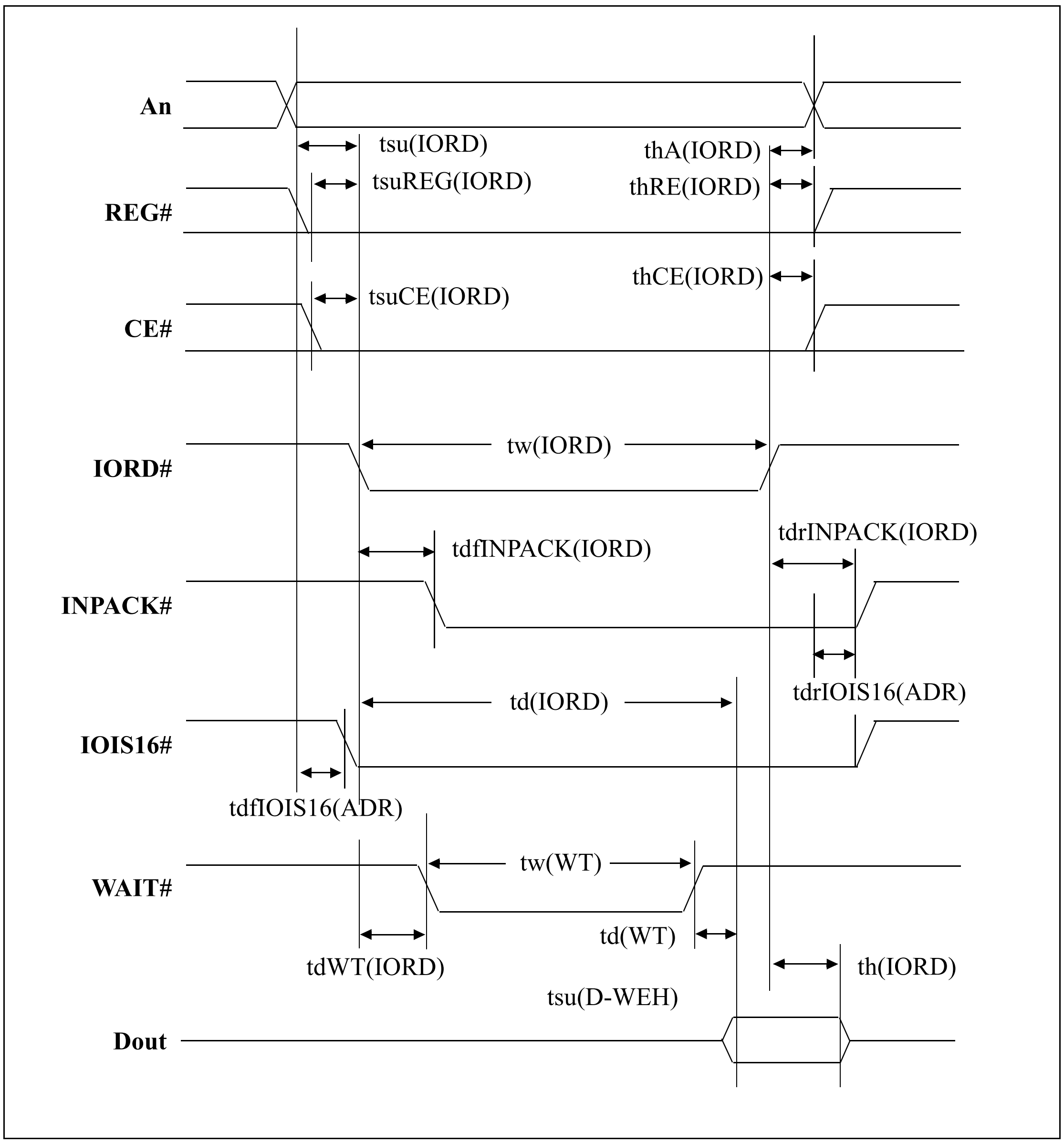
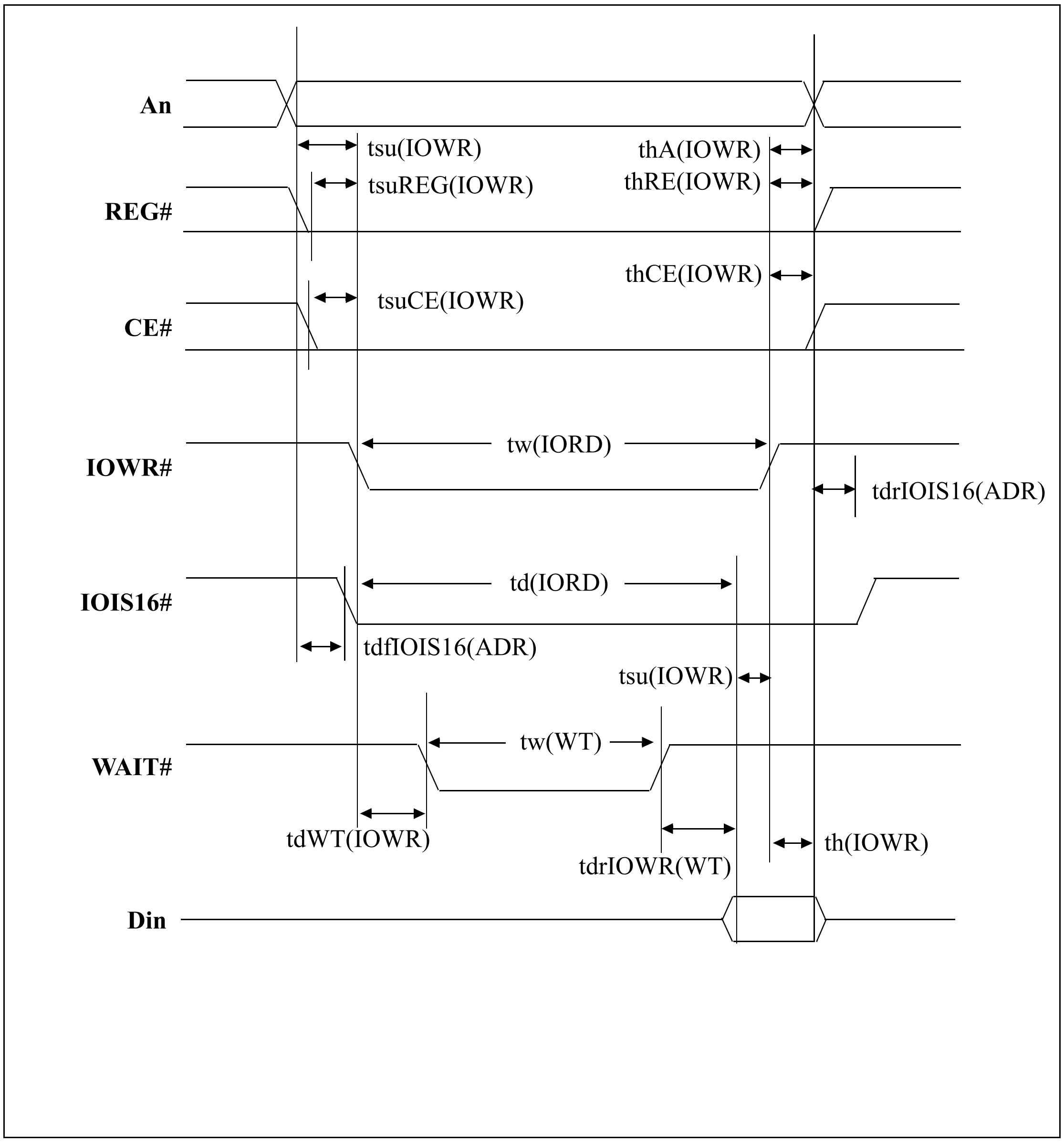
6.1.5 I/O Memory Read Timing Diagram



6.1.6 I/O Memory Write Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH		100
Data Hold following IOWR	th(IOWR)	tIWHDX	0	
IOWR Width Time	tw(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
REG setup before IOWR	tsuREG(IOWR)	tRGLIWL	5	
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35
Wait Delay Falling from IOWR	tdWT(IOWR)	tIWLWTL		35
IOWR high from Wait High	tdrIOWR(WT)	tWTJIWH	0	
Wait Width Time	tw(WT)	tWTLWTH		350

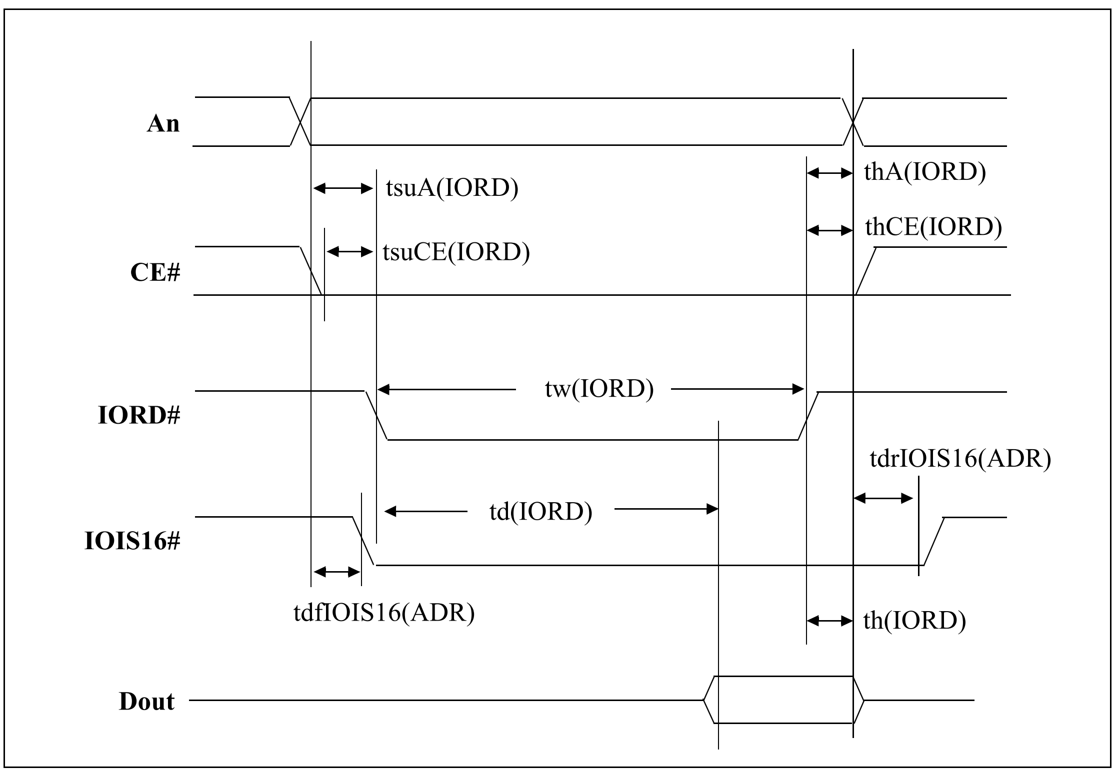
6.1.6 I/O Memory Write Timing Diagram



6.1.7 True IDE Mode Read Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Data Delay after IORD	td(IORD)	tIGLQV		100
Data Hold following IORD	th(IORD)	tIGHQX	0	
IORD Width Time	tw(IORD)	tIGLIGH	165	
Address Setup before IORD	tsuA(IORD)	tAVIGL	70	
Address Hold following IORD	thA(IORD)	tIGHAX	20	
CE setup before IORD	tsuCE(IORD)	tELIGL	5	
CE Hold following IORD	thCE(IORD)	tIGHEH	20	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35

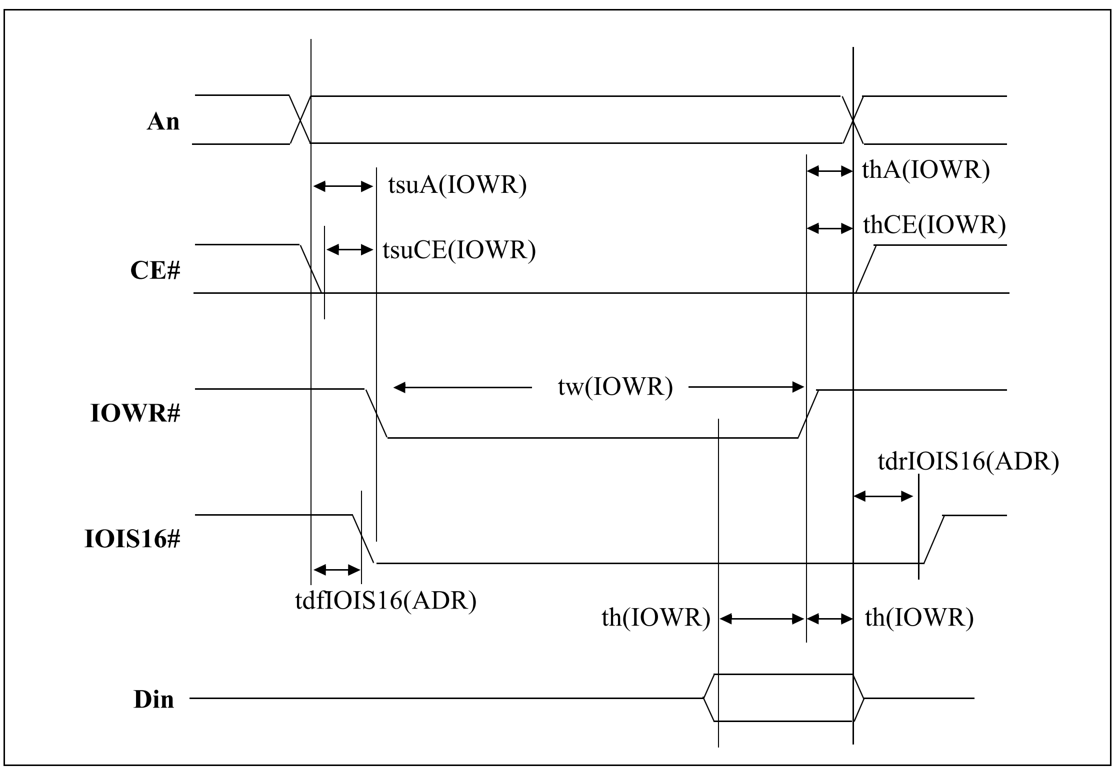
6.1.7 True IDE Mode Read Timing Diagram



6.1.8 True IDE Mode Write Timing

Item	Symbol	IEEEE Symbol	Min. (ns)	Max. (ns)
Data Setup before IOWR	tsu(IOWR)	tDVIWH		100
Data Hold following IOWR	th(IOWR)	tIWHDX	0	
IOWR Width Time	twl(IOWR)	tIWLIWH	165	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70	
Address Hold following IOWR	thA(IOWR)	tIWHAX	20	
CE setup before IOWR	tsuCE(IOWR)	tELIWL	5	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20	
IOIS16 Delay Assertion from Address	tdfIOIS16(ADR)	tAVISL		35
IOIS16 Delay Negation from Address	tdrIOIS16(ADR)	tAVISH		35

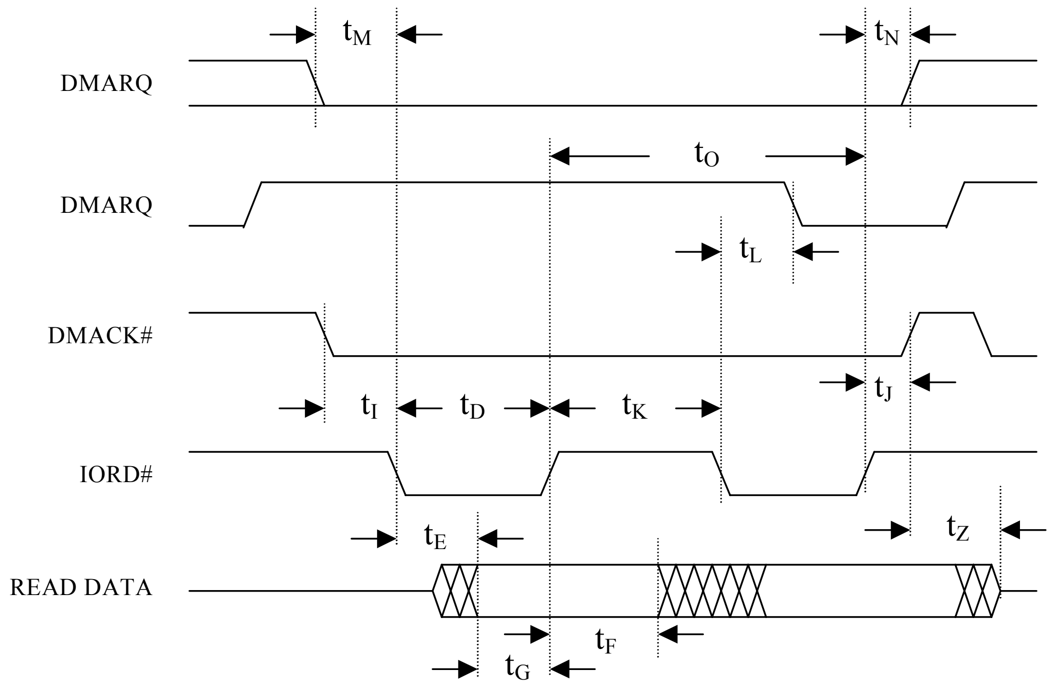
6.1.8 True IDE Mode Write Timing Diagram



6.1.8 True IDE DMA Mode Read Timing

Item	Symbol	Min. (ns)	Max. (ns)
Cycle Time	T_O		120
IORD asserted width	T_D	70	
IORD Data Access	T_E		50
IORD Data Hold	T_F	5	
IORD/IOWR Data Setup	T_G	20	
IOWR Data Hold	T_H	10	
DMACK to IORD/IOWR setup	T_I	0	
IORD/IOWR to DMACK hold	T_J	5	
IORD negated width	T_{KR}	25	
IOWR negated width	T_{KW}	25	
IORD to DMARQ delay	T_{LR}		35
IOWR to DMARQ delay	T_{LW}		35
CE valid to IORD/IOWR	T_M	25	
CE Hold	T_N	10	
DMACK	T_Z	25	

6.1.8 True IDE DMA Mode Read Timing Diagram



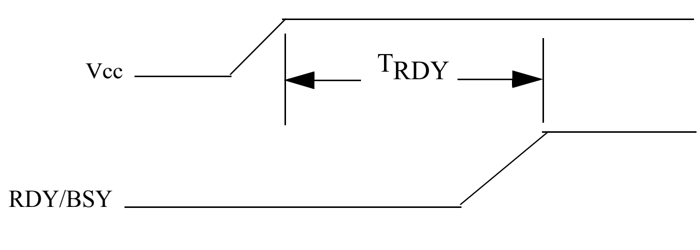
7.1 Electrical Characteristics

7.1.1 Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply Voltage	-0.3 ~7.0	V
V_{IN}	Input Voltage	GND - 0.5 to $V_{CC + 0.5}$	V
I_{IN}	DC Input Current	-10	mA
T_{STG}	Storage Temperature	-65 to 150	^oC

7.1.2 Recommended Operating Conditions

Symbol	Parameter		Ratings	Unit
V_{DD}	Supply Voltage	5.0V	4.5 to 5.5	V
		3.3V	3.15 to 3.45	V
T_A	Operating Temperature	Commercial	0 to 70	^oC
		Industrial	-40 to 85	^oC
T_{RDY}	Power on to Ready		100	ms



POWER ON TO READY

7.1.3 DC Electrical Characteristics

(T_A = 0 to 70 ^oC V_{DD} = 3.3V +/- 5%)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input Voltage	CMOS		2.0			V
V_{IL}	Low Level Input Voltage	CMOS				1.0	V
V_T	Switching Threshold	CMOS			1.4		V
V_{T+}	Switching Threshold, Positive going threshold	CMOS				2.0	V
V_{T-}	Switching Threshold, Negative going threshold	CMOS		1.0			V
I_{IH}	High Level Input Current	Input Buffer	$V_{IN} = V_{DD}$	-10		10	uA
		Input Buffer with pull-up		10	30	60	uA
I_{IL}	Low Level Input Current	Input Buffer	$V_{IN} = V_{SS}$	-10		10	uA
		Input Buffer with pull-up		-160	-30	-10	uA
V_{OH}	High Level Output Current	Type 4(1)	I_{OH} = -4mA	2.4			V
		Type 8(2)	I_{OH} = -8mA				
		Type 16(3)	I_{OH} = -16mA				
V_{OL}	Low Level Output Current	Type 4(1)	I_{OH} = 4mA			0.4	V
		Type 8(2)	I_{OH} = 8mA				
		Type 16(3)	I_{OH} = 16mA				
I_{OZ}	Tri-state leakage current		$V_{OUT} = V_{SS}$ or V_{DD}	-10		10	uA
I_{DD}	Maximum Operating Current		V_{DD} = 3.3V f_{CLK} = 20MHz		30	40	mA
I_{idle}	Idle current					20	mA
I_{ds}	Stop current					30	uA

Notes:
1. 4mA drive output
2. 8mA drive output
3. 16mA drive output

7.1.3 DC Electrical Characteristics (contd.)

(T_A = 0 to 70 ^oC V_{DD} = 5V +/- 10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High level Input Voltage	CMOS		3.5			V
		TTL		2.0			V
V_{IL}	Low Level Input Voltage	CMOS				1.5	V
		TTL				0.8	V
V_T	Switching Threshold	CMOS			2.5		V
		TTL			1.4		V
V_{T+}	Switching Threshold, Positive going threshold	CMOS				4.0	V
		TTL				2.0	V
V_{T-}	Switching Threshold, Negative going threshold	CMOS		1.0			V
		TTL		0.8			V
I_{IH}	High Level Input Current	Input Buffer	$V_{IN} = V_{DD}$	-10		10	uA
		Input Buffer with pull-up		10	50	100	uA
I_{IL}	Low Level Input Current	Input Buffer	$V_{IN} = V_{SS}$	-10		10	uA
		Input Buffer with pull-up		-100	-50	-10	uA
V_{OH}	High Level Output Current	Type 4(1)	I_{OH} = -4mA	2.4			V
		Type 8(2)	I_{OH} = -8mA				
		Type 16(3)	I_{OH} = -16mA				
V_{OL}	Low Level Output Current	Type 4(1)	I_{OH} = 4mA			0.4	V
		Type 8(2)	I_{OH} = 8mA				
		Type 16(3)	I_{OH} = 16mA				
I_{OZ}	Tri-state leakage current		$V_{OUT} = V_{SS}$ or V_{DD}	-10		10	uA
I_{DD}	Maximum Operating Current		V_{DD} = 3.3V f_{CLK} = 20MHz		60	70	mA
I_{idle}	Idle current					35	mA
I_{ds}	Stop current					60	uA

Notes: 1. 4mA drive output 2. 8mA drive output 3. 16mA drive output

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