

**Revision History**

<b>Rev</b>	<b>Date</b>	<b>Details</b>
A	January 4, 2006	Preliminary Release of SMART ATA Flash data sheet w/SM222 controller

---

## ***32MB – 4GB ATA Flash Cards***

### **1 General Description**

#### **1.1 Overview**

SMART is a leading independent manufacturer of memory and embedded modular sub-systems inclusive of board-level through systems level design, manufacturing, test and fulfillment services. We offer more than 500 standard and custom products to leading OEMs in the computer, industrial, networking and telecommunications industries worldwide.

SMART's high-performance ATA Flash Card product offering is specifically targeted at the needs of OEM markets such as networking, telecommunications and data communications applications. SMART's ATA products are also a natural fit for mobile and embedded computing, medical, automotive and industrial applications.

SMART's ATA products offer reliable high performance operation in an industry standard Type 1 ultrasonic welded PC Card housing. They are available in capacities from 32MB to 2GB and can operate in either 3.3V or 5V hosts.

Incorporating on-board error detection and correction algorithms and dynamic wear leveling techniques insure SMART's ATA product provides years of reliable operation over the life cycle. SMART further increases the reliability of its ATA product offering - yielding greater than 2 Million Program/Erase cycles for most applications - by using Single Level Cell NAND Flash technology which betters comparable Multi Level Cell technology by a factor of 10X in reliability and 2X in speed.

SMART has built its foundation by providing proven technology and quality products to the most demanding Fortune 100 OEMs. SMART engineers its products to perform at the highest degree of reliability & compatibility while backing these products with outstanding services and technology expertise.

#### **1.2 Features**

- PC Card Standard Release 8 Compliant
- Capacity Range 32MB to 4GB
- CIS (Card Information Structure) programmed into 256 Bytes of Attribute Memory
- Low Power Dissipation
  - High Performance Read Current: 30mA @ 5V, 30mA @ 3.3V
  - High Performance Write Current: 35mA @ 5V, 30mA @ 3.3V
  - Passive Mode: <7.5mA
- Supports Memory Mapped, I/O Mapped, and True IDE Interface Modes
- Supports up to PIO Mode 4 and DMA Multi-Word 2
- On-Board Wear Leveling
- RoHS compliant (Leaded optional)
- Industrial Temp Range -40°C to +85°C (Optional)

### 1.3 Part Numbering Information

SMART Part Number	Chip Density	Physical Capacity	Sector Card	Head	Cylinder	Sector Track	Un-Formatted Capacity
Sx9PC32SMB6y	256Mb	32MB	61,488	16	61	63	31,481,856
Sx9PC64SMB5y	512Mb	64MB	124,992	16	124	63	63,995,904
Sx9PC128SMB1y	1Gb	128MB	252,000	16	250	63	129,024,000
Sx9PC256SMB1y	1Gb	256MB	504,000	16	500	63	258,048,000
Sx9PC512SMB2y	2Gb	512MB	1,014,048	16	1006	63	519,192,576
Sx9PC1GSMB4y	4Gb	1GB	2,016,000	16	2000	63	1,032,192,000
Sx9PC2GSMB9y	8Gb	2GB	4,061,232	16	4029	63	2,079,350,784
Sx9PC4GSMB9y	8Gb	4GB	8,124,480	16	8060	63	4,159,733,760

x = Material Declaration

**G** -RoHS Complaint  
**M** -Standard Leded

y: Operating Temperature Range

**Blank** - Commercial  
**I** - Industrial

Note: Uses both Samsung and Hynix NAND

### 1.4 Part Number Decoder

<u>SG</u>	<u>9</u>	<u>PC</u>	<u>xxx</u>	<u>SMB</u>	<u>x</u>	<u>I</u>
SG - RoHS SM - Leded	Flash Memory	ATA Flash Card	32: 32MB 64: 64MB 128: 128MB 256: 256MB 512: 512MB 1G: 1GB 2G: 2GB 4G: 4GB	Controller SM222	6: 256Mb 5: 512Mb 1: 1Gb 2: 2Gb 4: 4Gb 9: 8Gb	Blank - Commercial I - Industrial

Note: Add 'FXD' extension for 'non-removable' drive

## 1.5 Specification Overview

### 1.5.1 Performance

▪ Maximum Performance (PIO 4)	<u>Read</u>	<u>Write</u>
256MB – 4GB	13MB/s	10MB/s
128MB	11MB/s	8MB/s
64MB	10MB/s	6MB/s
32MB	11MB/s	1.8MB/s
▪ Host Interface Transfer Rate	16MB/s	
▪ Startup Times		
Sleep to Read/Write	< 2.5ms	
Power up to Ready	< 200ms	
▪ Command to DRQ		
Read	< 200us	
Write	< 45us	

### 1.5.2 Reliability

▪ MTBF	> 2,500,000 hours
▪ Data Reliability	1 in 10 <sup>14</sup> bits, read
▪ Data Retention	10 years
▪ Endurance	>2,000,000 program/erase cycles

### 1.5.3 Power

▪ VCC	5.0V±10%	3.3V±5%
▪ Read	30mA	30mA
▪ Write	35mA	30mA
▪ Passive	7.5mA	1.5mA

### 1.5.4 Environmental

▪ Shock	50G max. @ 11ms
▪ Vibration	15G peak to peak
▪ Operating temperature	0°C to 70°C (Commercial) -40°C to +85°C (Industrial)
▪ Storage temperature	-65°C to 150°C
▪ Humidity	5% to 95%
▪ Altitude	up to 80,000 ft.

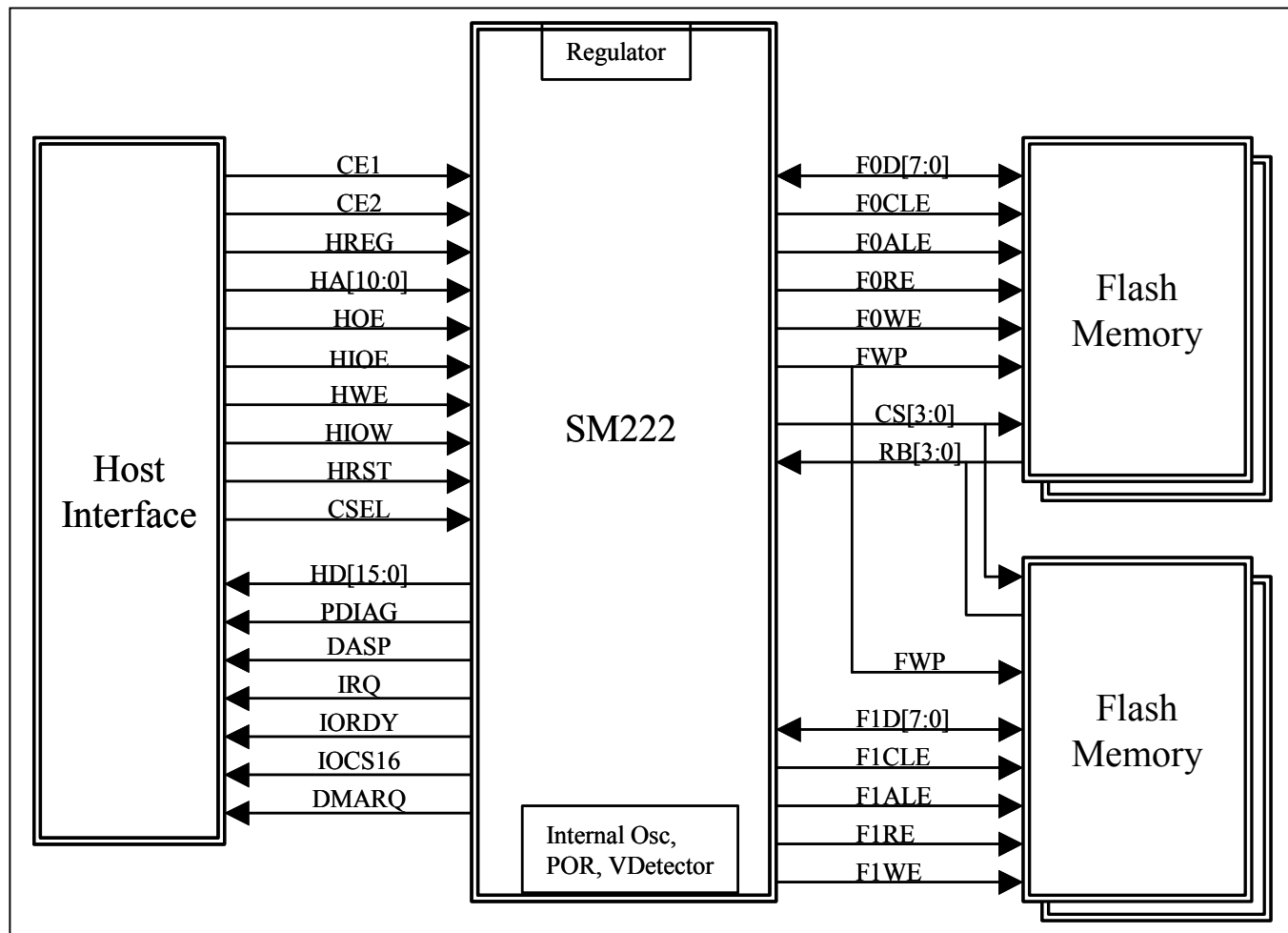
### 1.5.5 Physical Dimensions

▪ Length	3.370 in. (85.6 mm.)
▪ Width	2.126 in. (54.0 mm.)
▪ Thickness	0.130 in. (3.30 mm.)
▪ Weight	0.36 Oz. (10.2 gm)

## 2 General Description

The ATA Card contains an ATA/IDE controller and one or more flash memory devices. Smart ATA product line is offered in a UL approved Type I housing with a 68 pin connector. On board ATA/IDE controller interfaces with a host system allowing data to be written to and read from the flash memory devices.

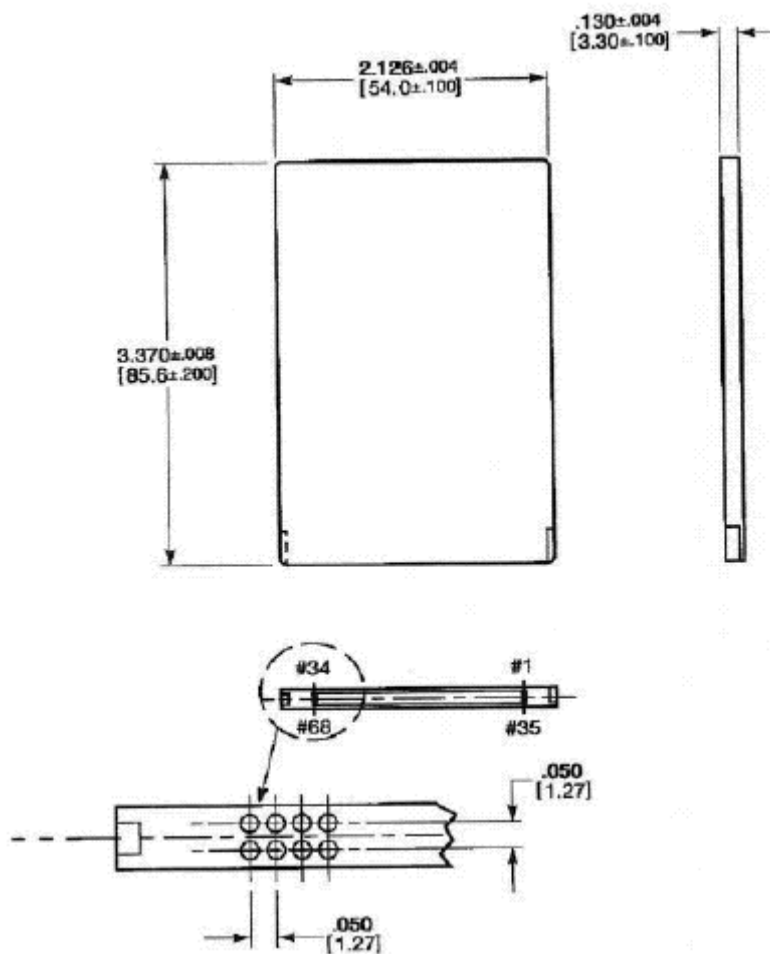
### 2.1 Functional Block Diagram



Notes:

All the signals shown going to the flash devices come from the card controller. All the other signals including those going to the card controller come from the Card Interface.

**2.2 Mechanical Specifications**



### **3 Electrical Interface**

#### **3.1 Electrical Description**

The Flash Cards are fully compliant with the ATA specification. This interface standard electrically complies with the PC Card ATA specifications, functioning in I/O Mode, Memory Mode and True IDE Modes.

Table 1 describes the I/O signals. Signals whose source is the host are designated as inputs (I) while signals that the ATA Flash Card sources are outputs (O). Bidirectional signals are designated as Input/Output (I/O). The ATA Flash Card logic levels conform to those specified in the PCMCIA Release 8 specification. Table 2 describes the signals in the three different operating modes of the card. The three modes are Card Memory, Card I/ O, and True IDE.

**Table 1. Pin Assignments and Pin Type**

Card Memory Mode			Card I/O Mode			True IDE Mode		
Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type
1	GND	Ground	1	GND	Ground	1	GND	Ground
2	D3	I/O	2	D3	I/O	2	D3	I/O
3	D4	I/O	3	D4	I/O	3	D4	I/O
4	D5	I/O	4	D5	I/O	4	D5	I/O
5	D6	I/O	5	D6	I/O	5	D6	I/O
6	D7	I/O	6	D7	I/O	6	D7	I/O
7	CE1#	I	7	CE1#	I	7	CS0#	I
8	A10	I	8	A10	I	8	A10	I
9	OE#	I	9	OE#	I	9	OE#	I
10	NC	I	10	A9	I	10	A9	I
11	A9	I	11	A8	I	11	A8	I
12	A8	I	12	A7	I	12	A7	I
13	NC	-	13	VCC	-	13	VCC	-
14	NC	I	14	A6	I	14	A6	I
15	WE#	I		WE#	I		WE#	I
16	RDY/BSY#	O		IREQ#	O		INTRQ	O
17	VCC	Power	51	VCC	Power	51	VCC	Power
18	NC	-	46	NC	-	46	NC	-
19	NC	-	46	NC	-	46	NC	-
20	NC	-	46	NC	-	46	NC	-
21	NC	-	46	NC	-	46	NC	-
22	A7	I		A7	I		A7	I
23	A6	I		A6	I		A6	I
24	A5	I	15	A5	I	15	A5	I
25	A4	I	16	A4	I	16	A4	I
26	A3	I	17	A3	I	17	A3	I
27	A2	I	18	A2	I	18	A2	I
28	A1	I	19	A1	I	19	A1	I
29	A0	I	20	A0	I	20	A0	I
30	D0	I/O	21	D0	I/O	21	D0	I/O
31	D1	I/O	22	D1	I/O	22	D1	I/O
32	D2	I/O	23	D2	I/O	23	D2	I/O
33	WP	O	24	IOIS16#	O	24	IOCS16#	O
34	GND	Ground	35	GND	Ground	35	GND	Ground



**Table 1. Pin Assignments and Pin Type (Continued)**

Card Memory Mode			Card I/O Mode			True IDE Mode		
Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type	Pin No.	Signal Name	Pin Type
35	GND	Ground	35	GND	Ground	35	GND	Ground
36	CD1#	O	36	CD1#	O	36	CD1#	O
37	D11	I/O	37	D11	I/O	37	D11	I/O
38	D12	I/O	38	D12	I/O	38	D12	I/O
39	D13	I/O	39	D13	I/O	39	D13	I/O
40	D14	I/O	40	D14	I/O	40	D14	I/O
41	D15	I/O	41	D15	I/O	41	D15	I/O
42	CE2#	I	42	CE2#	I	42	CS1#	I
43	VS1#	O	43	VS1#	O	43	VS1#	O
44	IORD#	I	44	IORD#	I	44	IORD#	I
45	IOWR#	I	45	IOWR#	I	45	IOWR#	I
46	NC	-	46	NC	-	46	NC	-
47	NC	-	47	NC	-	47	NC	-
48	NC	-	48	NC	-	48	NC	-
49	NC	-	49	NC	-	49	NC	-
50	NC	-	50	NC	-	50	NC	-
51	VCC	Power	51	VCC	Power	51	VCC	Power
52	NC	-	52	NC	-	52	NC	-
53	NC	-	53	NC	-	53	NC	-
54	NC	-	54	NC	-	54	NC	-
55	NC	-	55	NC	-	55	NC	-
56	NC	-	56	NC	-	56	CSEL#	I
57	VS2#	O	57	VS2#	O	57	VS2#	O
58	RESET	I	58	RESET	I	58	RESET#	I
59	WAIT#	O	59	WAIT#	O	59	IORDY	O
60	INPACK#	O	60	INPACK#	O	60	DREQ	O
61	REG#	I	61	REG#	I	61	DMACK#	I
62	BVD2	I/O	62	SPKR#	I/O	62	DASP#	I/O
63	BVD1	I/O	63	STSCHG#	I/O	63	PDIAG#	I/O
64	D8	I/O	64	D8	I/O	64	D8	I/O
65	D9	I/O	65	D9	I/O	65	D9	I/O
66	D10	I/O	66	D10	I/O	66	D10	I/O
67	CD2#	O	67	CD2#	O	67	CD2#	O
68	GND	Ground	68	GND	Ground	68	GND	Ground

**Table 2. Signal Description**

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
<b>CD1#,CD2#</b>		O	36,67	Card Detect Outputs
	Card Memory Mode			These Card Detect pins are connected to ground on the Card. They are used by the host to determine that the Card is fully inserted into the socket.
	Card I/O Mode			This signal is the same in this mode.
	True IDE Mode			This signal is the same in this mode.
<b>IOWR#</b>		I	45	I/O Write Input
	Card Memory Mode			This signal is not used in this mode.
	Card I/O Mode			The I/O Write strobe pulse is used to clock I/O data on the Card data bus into the controller registers. The clocking will occur on the negative to positive going edge of the signal.
	True IDE Mode			This signal has the same function as in Card I/O Mode.
<b>IORD#</b>		I	44	I/O Read Input
	Card Memory Mode			This signal is not used in this mode.
	Card I/O Mode			This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Card.
	True IDE Mode			This signal has the same function as in Card I/O Mode.
<b>WE#</b>		I	15	Write Enable Input
	Card Memory Mode			This is a signal driven by the host and used for strobing memory write data to the registers of the Card. It is also used for writing the configuration registers
	Card I/O Mode			In this mode, this signal is used to write the CIS and configuration registers
	True IDE Mode			In this mode, this input signal is not used and should be connected to VCC by the host.
<b>CSEL#</b>		I	56	Cable Select Input
	Card Memory Mode			This signal is not used in this mode.
	Card I/O Mode			This signal is not used in this mode.
	True IDE Mode			This signal is used to configure this device as Master or Slave. When this pin is grounded, this device is configured as Master. When this pin is tied to VCC this card is configured as Slave

**Table 2. Signal Description (continued)**

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
<b>OE#</b>		I	9	Output Enable Input
	Card Memory Mode			This is a strobe generated by the host interface. It is used to read data from the Card and to read the CIS and configuration registers
	Card I/O Mode			This signal is used to read the CIS and configuration registers only.
	True IDE Mode			To enable the True IDE Mode, this input should be grounded by the host.
<b>CE1#,CE2# / CS0#, CS1#</b>		I	7,42	Card Enable Inputs
<b>CE1#, CE2#</b>	Card Memory Mode			These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the odd byte of the word. CE1# accesses the even byte or the odd byte of the word depending on A0 and CE2#. A multiplexing scheme based on A0, CE1#, and CE2# allows 8 bit hosts to access all data on D0-D7
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
<b>CS0#, CS1#</b>	True IDE Mode			In the True IDE Mode, CS0# is the chip select for the ATA Command block registers while CS1# is used to select the ATA Control Block registers (Alternate Status Register and the Device Control Registers)
<b>WP/IOIS16# / IOCS16#</b>		O	33	Write Protect / I/O Port 16 Output
<b>WP</b>	Card Memory Mode			The card does not have a WP switch. This signal is held low after reset initialization sequence.
<b>IOIS16#</b>	Card I/O Mode			A low signal indicated that a 16 bit or odd byte only operation can be performed.
<b>IOCS16#</b>	True IDE Mode			This signal is asserted low when the card is expecting a word data transfer cycle. This open collector line is only driven on assertion (low).
<b>GND</b>		Power	1,34,35,68	Ground Pin
<b>VCC</b>		Power	17,51	Power Supply Pin

**Table 2. Signal Description (continued)**

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
<b>RESET / RESET#</b>		I	58	Card Reset Input
<b>RESET</b>	Card Memory Mode			When this pin is high, this signal resets the Flash Card. The card Reset is only at power-up if this pin is left high or open from power-up. The card is also reset when the Soft Reset bit in the Card Configuration Option Register is set
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
<b>RESET#</b>	True IDE Mode			In this mode, this input pin is active low from the host.
<b>D15-D0</b>		I/O	41,40,39,38,37,66,65,64,6,5,4,3,2,32,31,30	16-bit Data Input/Output Bus
	Card Memory Mode			These lines carry the Data, Commands, and Status Information between the host and the controller. D15 is the MSB of odd byte and D7 the MSB of even byte in a Word Access.
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
	True IDE Mode			All register operations occur in byte mode on D7-D0, while all data transfers are word (16-bit) accesses.
<b>A10-A0</b>		I	8,11,12,22,23,24,25,26,27,28,29	Card Address Input Bus
	Card Memory Mode			These addresses along with the REG# signal are used to select the following: the I/O port address registers in the card, the memory mapped port address registers, a byte in the CIS and Configuration Control and Status registers.
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
<b>A2-A0</b>	True IDE Mode			In this mode, only A2-A0 are used to select one of the Control/Status registers. All the remaining unused address lines should be grounded by the host. (grounded on the CF card also)

**Table 2. Signal Description (continued)**

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
<b>REG# / DMACK#</b>		I	61	Attribute Memory Select Input / DMA Acknowledge
<b>REG#</b>	Card Memory Mode			This signal is used to select between Register/Attribute Memory (REG# = low) and Common Memory (REG# = high)
<b>REG#</b>	Card I/O Mode			Active Low on this signal will allow accesses to I/O space
<b>DMACK#</b>	True IDE Mode			This is the DMA Acknowledge signal that is used for DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. This signal is used in a handshake manner with DREQ.
<b>RDY/BSY# / IREQ# / INTRQ</b>		O	16	Ready/Interrupt Request Output
<b>RDY/BSY#</b>	Card Memory Mode			This signal is set high when the card is ready to accept a new data transfer operation and held low when the card is busy. The host must have a pull-up resistor on this signal. When powering-up and when reset, the signal is held low (busy) until the card has completed the power-up or reset operation. When the signal indicates busy no operations to the card are permitted. The signal is held high whenever the card has been powered up with RESET# disconnected or asserted.
<b>IREQ#</b>	Card I/O Mode			In this mode, this signal is used as interrupt request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt. This is set using Configuration Option Register.
<b>INTRQ</b>	True IDE Mode			In this mode, the signal is active high request to the host.
<b>INPACK# / DREQ</b>		O	60	Input Port Acknowledge Output / DMA Request
<b>INPACK#</b>	Card Memory Mode			This signal is not used in this mode.
<b>INPACK#</b>	Card I/O Mode			This signal is asserted by the card when the card is selected and is responding to an I/O read cycle. This signal is used by the host to enable the input data buffers between the host and the card.
<b>DREQ</b>	True IDE Mode			This is the DMA Request that is used for the DMA data transfers between host and device. It shall be asserted by the device when it is ready to transfer data to or from the host. This signal is used in a handshake manner with DMACK#.

**Table 2. Signal Description (continued)**

Signal Name	Mode of Operation	Pin Type	Pin No(s).	Description
<b>WAIT# / IORDY</b>		O	59	Extend Bus Cycle / I/O Channel Ready Output
<b>WAIT#</b>	Card Memory Mode			This signal is driven low by the card to inform the host to delay completion of the cycle in progress.
	Card I/O Mode			This signal has the same function as in Card Memory Mode.
<b>IORDY</b>	True IDE Mode			This signal is held low to extend the host transfer of any host register access (read or write) when the card is not ready to respond to a data transfer request.
<b>BVD1 / STSCHG# / PDIAG#</b>		O	63	Battery Voltage Detect Output / Card Status Changed Output / Passed Diagnostics Input/Output
<b>BVD1</b>	Card Memory Mode			This signal is asserted high since the card does not contain a battery.
<b>STSCHG#</b>	Card I/O Mode			This signal is asserted low to alert the host to changes in the RDY/BSY# and Write Protect states. Its use is controlled through the Card Configuration and Status Registers
<b>PDIAG#</b>	True IDE Mode	I/O		This signal is asserted by slave drive to indicate to master drive that it has completed diagnostics and is ready to provide status.
<b>BVD2 / SPKR# / DASP#</b>		O	62	Battery Voltage Detect Output / Audio Waveform Output / Drive Active/Drive 1 Preset Output
<b>BVD2</b>	Card Memory Mode			This signal is asserted high since the card does not contain a battery
<b>SPKR#</b>	Card I/O Mode			This signal is asserted high since the card does not support audio.
<b>DASP#</b>	True IDE Mode	I/O		This signal indicates that a drive is active or that a slave drive (Drive 1) is present.
<b>VS1#, VS2#</b>		O	43,57	Voltage Sense Outputs
	Card Memory Mode			VS1# is grounded so that the Card's CIS can be read at 3.3V and VS2# is left open.
	Card I/O Mode			This signal is the same in this mode also.
	True IDE Mode			This signal is the same in this mode also.

**Table 3. Host Signal Termination**

<b>Item</b>	<b>Signal</b>	<b>Host</b>
Status Signal	<b>RDY/BSY#</b> <b>WAIT#</b> <b>WP</b>	Pull-up to Vcc R ≥ 10 KΩ
	<b>INPACK#</b>	In PCMCIA modes Pull-up to Vcc R ≥ 10 KΩ  In True IDE mode, if DMA operation is supported by the host, Pull-down to GND R ≥ 5.6 KΩ  PCMCIA / True IDE hosts switch the pull-up to pull-down in IDE mode if DMA operation is supported.  The PCMCIA mode Pull-up may be left active during True IDE mode if True IDE DMA operation is not supported.
Voltage Sense	<b>VS1</b> <b>VS2</b>	Pull up to VCC 10 KΩ ≤ R ≤ 100 KΩ
Battery/Detect	<b>BVD[2:1]</b>	Pull-up R ≥ 50 KΩ

## 3.2 Card Configuration

### 3.2.1 Registers and Memory Space Decoding

CE2#	CE1#	REG#	OE#	WE#	A10	A9	A8-A4	A3	A2	A1	A0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	X	1	XX	X	X	X	0	Configuration Register Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit – D7-D0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit – D15-D8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bit – D15-D0)
X	0	0	1	0	X	1	XX	X	X	X	0	Configuration Register Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit – D7-D0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit – D7-D0)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (8 bit – D7-D0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

### 3.2.2 Configuration Registers Decoding

CE2#	CE1#	REG#	OE#	WE#	A10	A9	A8-A4	A3	A2	A1	A0	Selected Space
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Register Read (200h)
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Register Write (200h)
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read (202h)
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write (202h)
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read (204h)
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write (204h)
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read (206h)
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write (206h)

Note: The location of the Card Configuration Registers should always be read from the CIS since these locations may vary in future products. No Writes should be performed to the Card Attribute Memory except to the Card Configuration Register Addresses. All other attribute memory locations are reserved.



### 3.3 Configuration Register Description

#### 3.3.1 Configuration Option Register (Address 200h in attribute memory)

The configuration Option Register is used to configure the card's interface, address decoding and interrupt and to issue a soft reset to the PC Card. This register is reset at System Power-On and by the RESET signal (after the flash card is configured in PC Card or ATA extension mode).

Operation	B7	B6	B5	B4	B3	B2	B1	B0
R/W	SRESET	LevlREQ	CONF5	CONF4	CONF3	CONF2	CONF1	CONF0

**SRESET** When this bit is set to logic one, the Host interface is in the reset state. This reset conditions is the same as a hardware or power-on reset state with the exception that this bit stays set, and the configuration as PCMCIA remains set. This software reset condition is removed when this bit is reset to logic zero. Following a power-on or hardware reset, this bit is cleared.

**LevlREQ** This bit is set to one for level mode interrupt and set to zero for pulse mode interrupt. In pulse mode interrupt, the pulse width is at least 0.5uS. In level mode interrupt, the interrupt line is low state until the interrupt is serviced by the system. The interrupt is driven in the inactive state.

**CONF5-CONF0** Configuration Index. Set to zero by reset. It's used to select operation mode of the Card as shown below. Please note that CONF5 and CONF4 are reserved and must be written as zero. See the table below.

CONF5	CONF4	CONF3	CONF2	CONF1	CONF0	Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, 16 contiguous registers
0	0	0	0	1	0	Primary I/O Mapped, 1F0-1F7/3F6-3F7
0	0	0	0	1	1	Secondary I/O Mapped, 170-177/376-377

**3.3.2 Card Status Register (Address 202h in attribute memory)**

This register contains information about the card's condition.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	Changed	SigChg	IOIs8	0	0	PwrDwn	Int	0
Write	0	SigChg	IOIs8	0	0	PwrDwn	0	0

- Changed** Indicates that one or both of the Pin Replacement Register CRdy, or CWProt bits are set to one.
- SigChg** This field serves as a gate for the STSCHG# signal. When the card is configured as I/O interface, and if this and the Changed field are set to one, the function shall assert STSCHG#. If this field is reset to zero, the card shall not assert STSCHG#.
- IOIs8** The host sets this bit to a one if the Card is to be configured in an 8 bit I/O mode. The control for an 8-bit data access is built into the ATA command set, and still must be used.
- PwrDwn** When the host sets this field to one, the card shall enter a power-down state. When this field is one, the host shall not access the card. The host shall return this field to zero before attempting to access the function. The host can set this function only if the card indicates it is ready. The RDY/BSY# value becomes busy when this bit is changed. RDY/BSY# will not become ready until the power state requested has been entered. The Card automatically powers down when it is idle and powers back up when it receives a command.
- Int** This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the IEN# bit in the device control register, this bit is a zero.

### 3.3.3 Pin Replacement Register (Address 204h in attribute memory)

This register provides status for signals on the CF Card interface that are used in Memory Access Mode but assume a different meaning or use in I/O Mode. The register may be read and written; however, when written, the lower four bits act as a mask for changing the corresponding upper four bits.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	0	0	CrDy/Bsy#	CWProt	0	0	Mrdy/Bsy	MWProt
Write	0	0	CrDy/Bsy#	CWProt	0	0	Mrdy/Bsy	MWProt

**CRdy/Bsy#** This bit is set to one when the bit RRdy/Bsy# changes state. This bit must be cleared by the host.

**CWProt** This bit is set to one when the RWprot changes state. This bit must be cleared by the host.

**RRdy/Bsy#** When read this bit represents the internal state of the RDY/BSY# signal. This bit may be used to read the state of RDY/BSY# as that pin has been reallocated to use as Interrupt Request when the card is configured as I/O interface.

**RWProt** This bit is always zero, since the card does not support a WP switch.

**MRdy/Bsy#** This bit acts as a mask for writing the corresponding CRdy/Bsy# bit.

**MWProt** This bit acts as a mask for writing the corresponding CWprot bit.

Initial value of "C" bit	Written by Host		Final value of "C" bit	Comment
	"C" Bit	"M" Bit		
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by host
X	1	1	1	Set by host

### 3.3.4 Socket and Copy Register (Address 206h in attribute memory)

This register contains additional configuration information. This register may be used by the host system to implement a substitute for the ATA Master/Slave functionality. This register is always written by the system before writing the card's Configuration Index register.

Operation	B7	B6	B5	B4	B3	B2	B1	B0
Read	Reserved	Copy Number			Socket Number			
Write	0	Copy Number			Socket Number			

**Reserved** This bit is reserved for future standardization. This bit must be set to zero by the software when the register is written.

**Copy Number** Drive's which indicate in their CIS that they support more than one copy of identically configured drive-cards, should have a copy number in this field. Only 0 or 1 is allowed

**Socket Number** This field indicates to the Flash Drive that it is located in the nth socket. The first socket is numbered 0.

## 3.4 Truth Tables (Transfer function tables)

### 3.4.1 Attribute Memory Table

REG#	CE2#	CE1#	A9	A0	OE#	WE#	D15-D8	D7-D0	Function Mode
X	1	1	X	X	X	X	High Z	High Z	Standby
0	1	0	0	0	0	1	High Z	Data	Read CIS (8 bits)
0	1	0	0	0	1	0	XX	Data	Write CIS (8 bits)
0	1	0	1	0	0	1	High Z	Data	Read Configuration Registers (8 bits)
0	1	0	1	0	1	0	XX	Data	Read Configuration Registers (8 bits)
0	0	0	0	X	0	1	Invalid	Data	Read CIS (16 bits)
0	0	0	0	X	1	0	XX	Data	Write CIS (16 bits)
0	0	0	1	X	0	1	Invalid	Data	Read Configuration Registers (16 bits)
0	0	0	1	X	1	0	XX	Data	Read Configuration Registers (16 bits)

Note: The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations.

### 3.4.2 Common Memory Table

The common memory accesses can be either 8 bit or 16 bit. The Card permits both 8 and 16 bit accesses to all of its common memory addresses.

The Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the WAIT# signal at the start of the cycle.

REG#	CE2#	CE1#	A0	OE#	WE#	D15-D8	D7-D0	Function Mode
X	1	1	X	X	X	High Z	High Z	Standby Mode
1	1	0	0	0	1	High Z	Even Byte	Byte Read (8 bits)
1	1	0	1	0	1	High Z	Odd Byte	
1	1	0	0	1	0	XX	Even Byte	Byte Write (8 bits)
1	1	0	1	1	0	XX	Odd Byte	
1	0	0	X	0	1	Odd Byte	Even Byte	Word Read (16 bits)
1	0	0	X	1	0	Odd Byte	Even Byte	Word Write (16 bits)
1	0	1	X	0	1	Odd Byte	High Z	Odd Byte Read (8 bits)
1	0	1	X	1	0	Odd Byte	XX	Odd Byte Write (8 bits)

### 3.4.3 I/O Interface Table

The I/O accesses can be either 8 bit or 16 bit. when a 16 bit port is addressed the signal IOIS16# is asserted by the PC card. Otherwise this signal is de-asserted. If on the other hand, when a 16-bit transfer is attempted and this signal is not asserted, the host must generate a pair of 8-bit references to access the even and odd bytes.

The Card may request the host to extend the length of a memory write cycle or extend the length of a memory read cycle until data is ready by asserting the WAIT# signal at the start of the cycle.

REG#	CE2#	CE1#	A0	IORD#	IOWR#	D15-D8	D7-D0	Function Mode
X	1	1	X	X	X	High Z	High Z	Standby Mode
0	1	0	0	0	1	High Z	Even Byte	Byte Input Access (8 bits)
0	1	0	1	0	1	High Z	Odd Byte	
0	1	0	0	1	0	XX	Even Byte	Byte Output Access (8 bits)
0	1	0	1	1	0	XX	Odd Byte	
0	0	0	0	0	1	Odd Byte	Even Byte	Word Input Access (8 bit)
0	0	0	0	1	0	Odd Byte	Even Byte	Word Output Access (8 bit)
1	X	X	X	0	1	XX	XX	I/O Read Inhibit
1	X	X	X	1	0	High Z	High Z	I/O Write Inhibit
0	0	1	X	0	1	Odd Byte	High Z	Odd Byte Input only (8 bits)
0	0	1	X	1	0	Odd Byte	XX	Odd Byte Output only (8 bits)

### 3.4.4 True IDE Mode Table

The Card can be configured in a True IDE Mode of operation. The Card can be configured in this mode only when the OE# signal is grounded by the host during the power off to power on cycle. In this True IDE Mode the Card protocol and configuration are disabled and only I/O operations to the task file and Data Registers are allowed. In this mode no memory or attribute registers are accessible to the host.

Removing ATA Flash Card and re-inserting the card while the host is powered-on will reconfigure the card into ATA mode from the original True IDE mode. To configure the card in the True IDE mode, the socket must be powered cycled with the Card inserted and the OE# asserted.

CE2#	CE1#	A2-A0	IORD#	IOWR#	D15-D8	D7-D0	Function Mode
0	0	X	X	X	High Z	High Z	Invalid
1	1	X	X	X	High Z	High Z	Standby Mode
1	0	1-7h	1	0	XX	Data In	Task File Write
1	0	1-7h	0	1	High Z	Data Out	Task File Read
1	0	0	1	0	Odd Byte in	Even Byte in	Data Register Write
1	0	0	0	1	Odd Byte out	Even Byte out	Data Register Read
0	1	6h	1	0	XX	Control In	Control Register Write
0	1	6h	0	1	High Z	Status Out	All Status Read

### 3.5 ATA Specific Register Mapping

The Card can be configured as a high performance I/O device through

- Standard PC-AT disk I/O address spaces 1F0h~1F7h, 3F6h~3F7h (primary), 170h~177h, 376h~377h (secondary) with IRQ14 (or other available IRQ).
- Any system decoded 16 byte I/O block using any available IRQ.
- Memory Space.

The communication to or from the Card is done using the Task File registers which provide all the necessary registers for control and status information. The Card interface connects peripherals to the host using four register mapping methods. The following is a detailed description of these methods:

Standard Configurations				
Config Index	I/O or Memory	Address	Drive#	Description
0 & 8	Memory	0-Fh, 400-7FFh	0	Memory Mapped
1 & 9	I/O	Xx0-xxFh	0	I/O Mapped 16 contiguous registers
2 & Ah	I/O	1F0h-1F7h, 3F6h-3F7h	0	Primary I/O Mapped Drive 0
2 & Ah	I/O	1F0h-1F7h, 3F6h-3F7h	1	Primary I/O Mapped Drive 1
3 & Bh	I/O	1F0h-1F7h, 3F6h-3F7h	0	Secondary I/O Mapped Drive 0
3 & Bh	I/O	1F0h-1F7h, 3F6h-3F7h	1	Secondary I/O Mapped Drive 1

### 3.5.1 Memory Mapped Addressing

When the Card registers are accessed via memory references, the registers appear in the common memory space window: 0~2K bytes as follows:

REG#	A10	A9-A4	A3	A2	A1	A0	Offset	OE# = 0	WE# = 0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	X	0	0	0	1	1	Error	Features	2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Duplicate Even RD Data	Duplicate Even WR Data	2
1	0	X	1	0	0	1	9	Duplicate Odd RD Data	Duplicate Odd WR Data	2
1	0	X	1	1	0	1	D	Duplicate Error	Duplicate Feature	2
1	0	X	1	1	1	0	E	Alternate Status	Device Control	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

Notes:

- Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
- Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Therefore, if the registers are byte accessed in the order 9 and then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.
- Accesses to even addresses between 400h and 7FFh access register 8. Accesses to odd addresses between 400h and 7FFh access register 9. This 1K byte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space. Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some Card adapters also have auto incrementing logic embedded within them. This address window allows these hosts and adapters to function efficiently. Note that this entire window accesses the Data Register FIFO and does not allow random access to the data buffer within the PC Card.



### 3.5.2 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CF Card, the registers are accessed in the block of I/O space decoded by the system as follows:

REG#	A3	A2	A1	A0	Offset	IORD# = 0	IOWR# = 0	Notes
1	0	0	0	0	0	Even RD Data	Even WR Data	1
1	0	0	0	1	1	Error	Features	2
1	0	0	1	0	2	Sector Count	Sector Count	
1	0	0	1	1	3	Sector No.	Sector No.	
1	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	1	1	1	7	Status	Command	
1	1	0	0	0	8	Duplicate Even RD Data	Duplicate Even WR Data	2
1	1	0	0	1	9	Duplicate Odd RD Data	Duplicate Odd WR Data	2
1	1	1	0	1	D	Duplicate Error	Duplicate Feature	2
1	1	1	1	0	E	Alternate Status	Device Control	
1	1	1	1	1	F	Drive Address	Reserved	

Notes:

- Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access. A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
- Register at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1. Therefore, if the registers are byte accessed in the order 9 and then 8 the data will be transferred odd byte then even byte. Repeated byte accesses to register 8 or 0 will access consecutive (even then odd) bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (even then odd) bytes from the data buffer. Byte accesses to register 9 access only the odd byte of the data.
- Address lines not indicated, are ignored by the Card for accessing all the registers in this table.

### 3.5.3 I/O Primary and Secondary Addressing

REG#	A9-A4	A3	A2	A1	A0	IORD# = 0	IOWR# = 0	Notes
0	1F(17)h	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)h	0	0	0	1	Error	Features	2
0	1F(17)h	0	0	1	0	Sector Count	Sector Count	
0	1F(17)h	0	0	1	1	Sector No.	Sector No.	
0	1F(17)h	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)h	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)h	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)h	0	1	1	1	Status	Command	
0	3F(37)h	0	1	1	0	Alternate Status	Device Control	
0	3F(37)h	0	1	1	1	Drive Address	Reserved	

Notes:

- Register 0 is accessed with CE1# and CE2# low as a word register on the combined odd data bus and even data bus. This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error/Feature byte-wide registers that lie at offset 1. When accessed twice at byte register with CE1# low, the first to be accessed is the even byte of the word and the second byte accessed is the odd byte of the equivalent word access.
- A byte access to register 0 with CE1# high and CE2# low accesses the error (when read) or feature (when written) register.
- Address lines which are not indicated are ignored by the Card for accessing all the registers in this table.

### 3.5.4 True IDE Mode Addressing

When the Card is configured in the True IDE mode, the I/O decoding is as follows:

CE2#	CE1#	A2	A1	A0	IORD# = 0	IOWR# = 0
1	0	0	0	0	Even RD Data	Even WR Data
1	0	0	0	1	Error	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control
0	1	1	1	1	Drive Address	Reserved

### 3.6 ATA Registers (Task File Registers)

The following section describes the hardware registers used by the host software to issue commands to the CF Card. These registers are often collectively referred to as the “Task File” registers.

Note: In accordance with the Card specifications, each of the registers which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15~D8) when CE1# is high and CE2# is low unless IOIS16# is high (not asserted) and I/O cycle is being performed.

#### 3.6.1 Data Register (Address – 1F0/170; offset – 0, 8, 9)

CE2#	CE1#	A0	Offset	Data Bus	Data Register
0	0	X	0, 8, 9	D15-D0	Word Data Register
1	0	0	0, 8	D7-D0	Even Data Register
1	0	1	9	D7-D0	Odd Data Register
0	1	X	8, 9	D15-D8	Odd Data Register
1	0	1	1, D	D7-D0	Error/Feature Register
0	1	X	1	D15-D8	Error/Feature Register
0	0	X	D	D15-D8	Error/Feature Register

The data register is a 16 bit register and it used to transfer data blocks between the Card data buffer and the host. This register overlaps the Error register.

The table above describes the combinations of data register access and is provided to assist in understanding the overlapped Data Register and Error/Feature Register rather than to attempt to define general Word and byte access modes and operations. See section 3.4 for various function transfer tables.

Note: Because of the overlapped register, access to the 1F1h and 171h or offset 1 are not defined for word (CE2# = 0 and CE1# = 0) operations. These accesses are treated as accesses to the Word Data Register. The duplicated registers at offsets 8h, 9h, Dh have no restrictions on the operations that can be performed by the socket.

### 3.6.2 Error Register (Address – 1F1/171; offset – 1, Dh; Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status Register. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with CE2# low and CE1# high.

- Bit 7 (BBK)            This bit is set when a Bad Block is detected. This bit is set when Error on Drive 1 (True IDE).
- Bit 6 (UNC)            This bit is set when an Uncorrectable Read Error is encountered.
- Bit 5                    This bit is set to 0.
- Bit 4 (IDNF)           The requested sector ID is in error or cannot be found.
- Bit 3                    This bit is set to 0.
- Bit 2 (ABRT)           This bit is set if the command has been aborted because card status: Not Ready, Write Fault, or when an invalid command has been issued.
- Bit 1                    This bit is set to 0.
- Bit 0 (AMNF)           This bit is set in case of a general error.

### 3.6.3 Feature Register (Address - 1F1/171; offset - 1, Dh; Write Only)

This register provides information regarding features of the Card that the host can utilize. This register is also accessed on data bits D15~D8 during a write operation to offset 0 with CE2# low and CE1# high.

### 3.6.4 Sector Count Register (Address - 1F2/172; offset - 2)

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the PC Card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred to complete the request.

### 3.6.5 Sector Number (LBA 7~0) Register (Address - 1F3/173; offset - 3)

This register contains starting sector number or bits 7~0 of the Logical Block Address (LBA) for any Card data access for the subsequent command.

### 3.6.6 Cylinder Low (LBA 15~8) Register (Address - 1F4/174; offset - 4)

This register contains the low order 8 bits of the starting cylinder address or bits 15~8 of the Logical Block Address (LBA).

**3.6.7 Cylinder High (LBA 23~16) Register (Address - 1F5/175; offset - 5)**

This register contains the high order 8 bits of the starting cylinder address or bits 23~16 of the Logical Block Address (LBA).

**3.6.8 Drive/Head (LBA 27~24) Register (Address - 1F6/176; offset - 6)**

The Drive/Head register is used to select the drive and head. It is also used to select the LBA addressing instead of cylinder/ head/sector addressing. The bits are defined as follows:

<b>B7</b>	<b>B6</b>	<b>B5</b>	<b>B4</b>	<b>B3</b>	<b>B2</b>	<b>B1</b>	<b>B0</b>
1	LBA	1	DRV	HS3	HS2	HS1	HS0

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with CE2# low and CE1# high.

- Bit 7                      This bit is set to 1.
- Bit 6 (LBA)              LBA is a flag to select either cylinder/head/sector (CHS) or LBA Mode. When this bit is zero, CHS mode is selected. When this bit is one, LBA mode is selected. In LBA Mode, the LBA is interpreted as follows:  
 LBA7~LBA0: Sector Number Register D7~D0  
 LBA15~LBA8: Sector Number Register D7~D0  
 LBA23~LBA16: Sector Number Register D7~D0  
 LBA27~LBA24: Sector Number Register HS3~HS0
- Bit 5                      This bit is set to 1.
- Bit 4 (DRV)              DRV is the drive number. When DRV is zero, drive/card 0 is selected. When DRV is one, drive/card 1 is selected. The Card is set to be card 0 or 1 using the copy field (Drive#) of the Card Socket & Copy configuration register.
- Bit 3 (HS3)              When operating in the CHS mode, this is bit 3 of the head number. It is Bit 27 when in LBA mode.
- Bit 2 (HS2)              When operating in the CHS mode, this is bit 2 of the head number. It is Bit 26 when in LBA mode.
- Bit 1 (HS1)              When operating in the CHS mode, this is bit 1 of the head number. It is Bit 25 when in LBA mode.
- Bit 0 (HS0)              When operating in the CHS mode, this is bit 0 of the head number. It is Bit 24 when in LBA mode.

**3.6.9 Status & Alternate Status Register (Address - 1F7/177 & 3F6/376; offset - 7, Eh; Read only)**

This register returns the Card status when read by the host. Reading the status register does clear a pending interrupt while reading the alternate status register does not. The status and alternate status registers are read only registers. When writing to the address of the status register command register is written. When writing to the address of the alternate status register, device control register is written. The status bits are defined as follows:

<b>B7</b>	<b>B6</b>	<b>B5</b>	<b>B4</b>	<b>B3</b>	<b>B2</b>	<b>B1</b>	<b>B0</b>
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR

- Bit 7 (BUSY)      When the busy bit is set, the controller is executing a command. Also, when this bit is set, the host may not read or write any other register except the Status, Alternate Status, Device Control, or Drive Address registers. This bit is set when RESET# is asserted. It is also set when an AT host sets Device Control Register, Bit 2 or when the Command registers is loaded by the host.
- Bit 6 (RDY)      RDY indicated whether the device is capable of performing Card operations. This bit is cleared at power up and remains cleared until the Card is ready to accept a command.
- Bit 5 (DWF)      This bit, if set, indicates a write fault has occurred.
- Bit 4 (DSC)      This bit is set when the Card is ready. This bit is cleared at power up.
- Bit 3 (DRQ)      The bit is set when the Card requires that information be transferred either to or from the host through the data register.
- Bit 2 (CORR)      This bit is set when a correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation. This bit is cleared when the Command register is written.
- Bit 1              This bit is always set to 0.
- Bit 0 (ERR)      This bit is set when the previous command has ended in some type of error. The bits in the error register contain additional information describing the error. This bit is cleared when the Command register is written.

**3.6.10 Command Register (Address - 1F7/177; offset - 7; Write only)**

The Command register contains the command code being sent to the device. Command execution begins immediately after this register is written. The Command register is a write only register. When reading from the address of the Command register, the Status register is read.

**3.6.11 Device Control Register (Address - 3F6/376; offset - Eh; Write only)**

This register is used to control the Card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the card is BUSY. The bits are defined as follows:

B7	B6	B5	B4	B3	B2	B1	B0
X	X	X	X	HD3En	SW Rst	IEn#	0

- Bit 7 – Bit 4            These bits are don't care. But it is recommended that the user program these bits to zero.
- Bit 3 (HD3En)        This bit is set to enable bit 3 of the address of the selected drive head giving a 4-bit addressable range corresponding to 1 to 16 heads.
- Bit 2 (SW Rst)        This bit is set to one in order to force the Card to perform an AT Disk controller soft reset operation. This does not change the Card configuration registers as hardware reset does. The card remains in reset until this bit is reset to zero.
- Bit 1 (IEn#)            The interrupt enable bit enables interrupts when the bit is zero. When this bit is set to one, interrupts from the Card are disabled. This bit also controls the Int bit in the configuration and status register. This bit is set to one at power on and reset.
- Bit 0                    This bit is ignored by the ATA Flash storage card

**3.6.12 Drive Address Register (Address - 3F7/377; offset - Fh; Read only)**

This is a diagnostic loop back register that contains Write Gate, Head Select3/Reduced Write Current, Head Select 2, Head Select 1, Head Select 0, Drive Select Drive 1, and Drive Select Drive 0. These bits reflect the state of the signals on the control cable. The host may read this register at any time. When host reads this register, only bits 6:0 are driven, bit 7 is High Impedance. NOTE: The Drive Address Register, also referred to as the Digital Input Register, is no longer supported in the ATA specifications. However, for backward compatibility, the ATA Flash Cards still supports this register, and responds as described.

B7	B6	B5	B4	B3	B2	B1	B0
HiZ	Wgate	H3/RWC	H2	H1	H0	DS1	DS0

## **4 ATA Command Description**

This section documents the Host Interface Commands supported by the Flash Card Controller. Two standard classes of interface specifications are currently implemented: the AT Attachment interface specifications and the PC Card specifications when operating in the PC Card Mode and the ATA specifications when operating in the true IDE mode.

Each command is discussed in terms of the contents of the Task File when the command is issued, the contents of the Task File when the host read the status after the command is completed, as well as the data that is transferred in response to the command issued.



### 4.1 ATA Command Set

The table below summarizes the ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

ATA Specification type	Command	Code
O	Check Power Mode	E5h or 98h
M	Executive Drive Diagnostic	90h
V	Erase Sector(s)	C0h
M	Format Track	50h
O	Identify Drive	Ech
O	Idle	E3h or 97h
O	Idle Immediate	E1h or 95h
M	Initialize Drive Parameters	91h
O	Read Buffer	E4h
M	Read Long Sector	22h or 23h
O	Read Multiple	C4h
M	Read Sector(s)	21h
M	Read Verify Sectors	40h or 41h
M	Recalibrate	1Xh
V	Request Sense	03h
M	Seek	7Xh
O	Set Features	Efh
O	Set Multiple Mode	C6h
O	Set Sleep Mode	E6h or 99h
O	Stand By	E2h or 96h
O	Stand By Immediate	E0h or 94h
V	Translate Sector	87h
V	Wear Level	F5h
O	Write Buffer	E8h
M	Write Long Sector	32h or 33h
O	Write Multiple	C5h
V	Write Multiple w/o Erase	CDh
M	Write Sectors(s)	30h or 31h
V	Write Sector(s) w/o Erase	38h
O	Write Verify	3Ch

Note:

- Type Abbreviation  
 M - Mandatory Command  
 O - Optional Command  
 V - Vendor Unique Command
- These type abbreviations pertain to the ATA Specifications only. In the case of CompactFlash-ATA specifications, all Host commands listed here are Mandatory.

## 4.2 ATA Command Set Definition

This section details the functionality of commands supported by the Flash Card. For each command, the Command Block register contents for the command invoked by the Host, and the Command Block registers updated by the Flash Card after command completion, are shown. Following is an example of the command description, showing the conventions used for each command description. Throughout this document, the terms ‘Task File’ and ‘Command Block’ are used interchangeably to refer to the ATA I/O registers

A detailed description of the execution of the command is provided. This is followed by two tables, the first showing the requirements of the Command Block registers at the time that the Host issues the command to the Flash card, and the second showing the contents of the Command Block after completion or termination on error of the command.

Command Block Specified by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	Command Code							
DRIVE/HEAD	nu	L	nu	D	H[3:0] or LBA[27:24] of the starting sector/LBA			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the first sector/LBA to transfer							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the first sector/LBA to transfer							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the first sector/LBA to transfer							
SECTOR COUNT	The number of sectors/logical blocks to transfer							
FEATURES	Set Features Code							

The preceding table represents the contents of the Command Block registers when the command is issued by the Host. Where applicable, the Host first writes the appropriate data into the Features, Sector Count, Sector Number, Cylinder Hi/Low, and Drive/Head registers, and lastly, writes the command code into the Command register. The act of writing to the command register causes the Flash card to execute the command based on the contents of the Command Block at that instance.

Note that bits 7 and 5 of the Drive/Head register are denoted as ‘nu.’ Although the Host is expected to always set these bits to 1 when the command is issued, the Flash card ignores the value of these bits.

Command Block specified by Flash card upon completion/termination of 'Sample' command								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	V	0	V
DRIVE/HEAD	na	na	na	D na	H[3:0] or LBA[27:24] of the last good sector transferred			
CYLINDER HI	Cylinder[15:8] or LBA[23:16] of the last good sector transferred							
CYLINDER LOW	Cylinder[7:0] or LBA[15:8] of the last good sector transferred							
SECTOR NUM	Sector[7:0] or LBA[7:0] of the last good sector transferred							
SECTOR COUNT	The number of sectors that were not transferred if an unrecoverable error occurred							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TKON F	AMNF
	V	V	0	V	0	V	0	0

The above table represents the contents of the Command Block registers upon completion of the command by the Flash card.

At the completion of every command, specific bits in the Status register is as follows: the BuSY, DriveWriteFault, DataReQuest, and InDeX bits are always de-asserted, while the DriveReaDY, and DriveSeekComplete bits are always asserted. The CORReCted ECC bit and the ERRor bit are set or cleared as appropriate.

The contents of the Error register are always set to zero when a command is received, and are only valid if the ERR bit in the Status register is set to '1' at the completion of a command. In addition, the MediaChange, MediaChangeRequest, TracK0NotFouNd, and AddressMarkNotFouNd bits are always cleared, regardless of the state of the ERR bit in the Status register.

For the Command Block tables, explanations for each possible code are shown below:

L (LBA Mode bit)	This bit is used to specify whether the requested sector is addressed in the LBA mode or in the Cylinder-Head-Sector, CHS, mode. When set, the LBA mode is specified. The LBA is comprised of the lower significant nibble in the Drive/Head register, LBA[27:24], concatenated with the contents of the Cylinder Hi/Lo, and the Sector registers, LBA[23:0], respectively. If L=0, the sector is addressed in the classic Cylinder/Head/Sector CHS mode.
D (Drive Select bit)	This bit is used to select card 0 or 1, allowing up to two cards to share a single Task File. If two PC Card ATA cards are present in the system, one of the cards may be assigned as copy 0, and the second card may be assigned as copy 1, using the Copy field of the PCMCIA Socket & Copy card configuration register. In this case, the card designated as Copy 0 is selected when D=0. Conversely, the card designated as Copy 1 is selected when D=1.
1 (Bit is Set)	When referring to the Command Block registers when the Host issues a command, this bit must be set to a 1 by the Host before command invocation.  When referring to the Command Block contents read by the Host after completion of a command, this bit is set by the Flash card upon command completion.
0 (Bit is Cleared)	When referring to the Command Block registers when the Host issues a command, this bit must be cleared to 0 by the Host before command invocation.  When referring to the Command Block contents read by the Host after completion of a command, this bit is cleared by the Flash card upon command completion.
nu (Not Used)	Although the Host may specify this register/bit when invoking the command, the value for this command block register or bit is ignored by the card.
V (Valid Data)	When referring to the Command Block contents read by the Host after completion of a command, the value for the applicable bit is specified by the card.
na (Not Affected)	The value for this bit, or register, is neither set nor cleared by the card; i.e., it is unchanged by the card after command completion.

### 4.3 Identify Drive Definition

This command passes to the Host one sector of data describing the Flash card's parameters. See Table for a detailed description of the Identify Drive data.

Identify Drive Command Issued by Host								
Task File Register	7	6	5	4	3	2	1	0
COMMAND	ECh							
DRIVE/HEAD	nu	nu	nu	D	nu			
CYLINDER HI	nu							
CYLINDER LOW	nu							
SECTOR NUM	nu							
SECTOR COUNT	nu							
FEATURES	nu							

Command Block specified by Flash card upon completion/termination of Identify Drive command (50h)								
Task File Register	7	6	5	4	3	2	1	0
	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR
STATUS	0	1	0	1	V	0	0	V
DRIVE/HEAD	na	na	na	na	na			
CYLINDER HI	na							
CYLINDER LOW	na							
SECTOR NUM	na							
SECTOR COUNT	na							
ERROR	BBK	UNC	MC	IDNF	MCR	ABRT	TKONF	AMNF
	0	0	0	0	0	0	0	0

<b>Identify Drive Information</b>		
Word	Data	Description
0	848Ah	General configuration bit-significant information
1	Note 1	Number of Cylinders
2	0000h	Reserved
3	Note 1	Number of Heads
4-5	0000h	Obsolete
6	Note 1	Number of sectors per track
7-8	0000h 0000h	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	0000h	Obsolete
10-19	XXXXh	20 ASCII char serial number. Words 10-19 are filled with 20 ASCII 'space' chars.
20	0002h	Obsolete
21	0002h	Obsolete
22	0004h	Number of ECC bytes passed on Read/Write Long Commands
23-26	xxxx	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	[Manufacturer's info]	Model: SMART CF
47	0001h	Maximum number of sectors on Read/Write Multiple command
48	0000h	Reservd
49	0300h	Capabilities: LBA supported, DMA supported
50	0000h	Reserved
51	0200h	PIO data transfer cycle timing mode
52	0000h	Obsolete
53	0003h	Words 54-58 are valid
54	Note 1	Number of Current Cylinders
55	Note 1	Number of Current Heads
56	Note 1	Number of Current Sectors Per Track
57-58	Note 1	Current Capacity in Sectors Word 57 = LSW, Word 58 = MSW
59	0101h	Current Setting for Block Count=1 for R/W Multiple Commands
60-61	Note 1	Total number of user addressable LBA's
62	0000h	Reserved
63	0407h	Multiword DMA mode 2 selected, Mode 0,1, & 2 supported
64	0003h	Advanced PIO modes supported
65	0050h	Minimum Multiword DMA transfer cycle time per word
66	0050h	Recommended Multiword DMA transfer cycle time
67	0050h	Minimum PIO transfer cycle time without flow control

<b>Identify Drive Information (cont)</b>		
Word	Data	Description
68	0050h	Minimum PIO transfer cycle time with IORDY flow control
69-81	0000h	Reserved
82-84	XXXXh	Features/command sets supported
85-87	XXXXh	Features/command sets enabled
88	0000h	Reserved
89	0000h	Time required for Security erase unit completion
90	0000h	Time required for Enhanced Security erase unit completion
91	0000h	Current Advanced power management value
92-127	0000h	Reserved
128	0000h	Security status
129-159	0000h	Vendor unique bytes
160	0000h	Power requirement description
161	0000h	Reserved for assignment by the CFA
162	0000h	Key management schemes supported
163-175	0000h	Reserved for assignment by the CFA
176-255	0000h	Reserved

Note 1: This value is dependent upon the total capacity of the specific flash card.

**5 Card Information Structure**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
00h	01	CISTPL_DEVICE								Device Info Tuple	Tuple Code
02h	04	CISTPL_LINK								Link is 4 bytes	Link to next Tuple
04h	DF	Device Type Code Dh = I/O				W 1	Device Speed 111			I/O Device, No WP Speed=Extended	Device ID WPS, Device Speed
06h	79	X	F == 8.0			1 = 10 ns			80 nsec	Extended Speed	
08h	01	00h == 1x				1 == 2k			2KB of address space	Device Size	
0Ah	FF	List End Marker								End of Devices	End Marker
0Ch	1C	CISTPL_DEVICE_OC								Device other condition Tuple	Tuple Code
0Eh	05	CISTPL_LINK								Link is 5 bytes	Link to next Tuple
10h	02	Reserved 0						3 1	W 0	3.3V operation Wait not used	3.3V operation
12h	DF	Device Type Code Dh = I/O				W 1	Device Speed 111			I/O Device, No WP Speed=Extended	Device ID WPS, Device Speed
14h	79	X	F == 8.0			1 = 10 ns			80 nsec	Extended Speed	
16h	01	00h == 1x				1 == 2k			2KB of address space	Device Size	
18h	FF	List End Marker								End of Devices	End of Marker
1Ah	18	CISTPL_JEDEC_C								JEDEC ID Common Memory	Tuple Code
1Ch	02	CISTPL_LINK								Link is 2 bytes	Link to next Tuple
1Eh	DF	PCMCIA Manufacturer's ID									Byte 1, JEDEC ID of Device 1
20h	01	PCMCIA Code for PC card ATA no Vpp Required								Second Byte of JEDEC ID	Byte 2 JEDEC ID
22h	20	CISTPL_MANFID								Manufacturing ID	Tuple Code
24h	04	CISTPL_LINK								Link is 4 bytes	Link to next Tuple
26h	7F	Card Manufacturer's Code								Smart JEDEC Manufacturer's ID	TPLMID_MANF
28h	94										TPLMID_MANF
2Ah	07	Manufacturer's Information									TPLMID_MANF
2Ch	00										TPLMID_MANF



### Card Information Structure (cont)

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
2Eh	15	CISTPL_VERS_1								Level 1 version	Tuple Code
30h	23	CISTPL_LINK								Link is 33 bytes	Link to next Tuple
32h	04	TPPLV_MAJOR								PCMCIA 2.0/ JEIDA 4.1	Major Version
34h	01	TPPLV_MINOR								PCMCIA 2.0/ JEIDA 4.1	Minor Version
36h	53	ASCII Manufacturing String								S	Info String 1
38h	4D									M	
3Ah	41									A	
3Ch	52									R	
3Eh	54									T	
40h	20										
42h	4D									M	
44h	4F									O	
46h	44									D	
48h	55									U	
4Ah	4C									L	
4Ch	41									A	
4Eh	52									R	
50h	20										
52h	54									T	
54h	45									E	
56h	43									C	
58h	48									H	
5Ah	00									.	
5Ch	53									S	
5Eh	4D									M	
60h	41									A	
62h	52									R	

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
68h	32									2	
6Ah	32									2	
6Ch	32									2	
6Eh	20										
70h	50									P	
72h	43									C	
74h	00									.	
76h	FF	List End Marker								End of Devices	End of Marker
78h	21	CISTPL_FUNCID								Control ID Tuple	Tuple Code
7Ah	02	CISTPL_LINK								Link is 2 bytes	Link to next Tuple
7Ch	04	IC Card Function Code								FIXED DISK Function	TPLFID_FUNCTION
7Eh	01	R0	R0	R0	R0	R0	R0	R0	P1	Attempt installation at Post P: Install at POST R: Reserved	
80h	22	CISTPL_FUNCCE								Function Extension Tuple	Tuple Code
82h	02	CISTPL_LINK								Link is 2 bytes	Link to next Tuple
84h	01	Disk Function Extension Tuple Type								Disk Device interface	TPLFE_TYPE

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
86h	01	Interface Type Code								PC Card-ATA interface	TPLFE_DATA
88h	22	CISTPL_FUNCE								Function Extension Tuple	Tuple Code
8Ah	03	CISTPL_LINK								Link is 3 bytes	Link to next Tuple
8Ch	02	Disk Function Extension Tuple Type								PCMCIA-ATA Extension Tuple	Extension Tuple Type for Disk
8Eh	0C	R 0	R 0	R 0	R 0	U 1	S 1	V 0		Silicon Drive V:0 No Vpp required S:Silicon U:ID Drive not Mfg/SN unique R:Reserved	TPLFE_DATA
90h	0F	R 0	I 0	E 0	N 0	P3 1	P2 1	P1 1	P0 1	Sleep, Standby, Idle Mode supported P0: Sleep Mode supported P1: Standby Mode supported P2: Idle Mode supported P3: Drive Auto Power Control not supported N: Same Primary or Secondary I/O addressing exclude 3F7H E: Index bit Not Emulated I: IOIS16 is asserted on Twin configuration R: Reserved	
92h	1A	CISTPL_CONFIG								Configuration Tuple	Tuple Code
94h	05	CISTPL_LINK								Link is 5 bytes	Link to next Tuple

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
96h	01	RFSZ 00		RMSZ 0000			RASZ 01			Size of Field RFSZ:reserved Field RMSZ: Reg Mask RASZ: Base Address	TPCC_SZ
98h	03	TPCC_LAST								Entry Index 03h	Last entry of Configuration table
9Ah	00	TPCC_RADR (LSB)								Configuration Registers are located at 200h	Location of Config Registers
9Ch	02	TPCC_RADR (MSB)									
9Eh	0F	R 0	R 0	R 0	R 0	S 1	P 1	C 1	I 1	4 Configuration registers are present I: Configuration Index C: Configuration & Status P: Pin replacement S: Socket and Copy R: Reserved for future	TPCC_RMSK
A0h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
A2h	08	CISTPL_LINK								Link is 8 bytes	Link to next Tuple
A4h	C0	I 1	D 1	Configuration Index 000000						Memory Mapped I/O D: Default Configuration I: Interface Byte Follows	TPCE_INDEX
A6h	C0	W 1	R 1	P 0	B 0	Interface Type 0000				Interface: Memory only BVD & WP not used, RDY/BSY# & Wait# used for Memory Cycle B: Battery Volt detects P: Write Protect R: RDY/BSY# W: Wait used for Memory Cycle	TPCE_IF
A8h	A1	M 1	MS 01	IR 0	IO 0	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info not present I/O: I/O port info not present IR: Interrupt info not present MS: Mem space info type M: misc. info bytes present	TPCE_FS	

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
AAh	01	R 0	DI 0	PI 0	AI 0	SI 0	HV 0	LV 0	N V1	Nominal operating supply voltage. NV: Nominal Voltage	Power Parameters for Vcc
ACh	55	X 0	Ah = 5.0				5h = 1V			Vcc Nominal is 5 Volts	Vcc Nominal Value
A Eh	08	Length in 256 byte pages (LSB)								Length of Mem Space is 2KB	TPCE_MS Length LSB
B0h	00	Length in 256 byte pages (MSB)								Start at 0 on card	TPCE_MS Length MSB
B2h	20	X 0	R 0	P 1	RO 0	A 0	Twin 0			Power Down T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc. Features	TPCE_MI
B4h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
B6h	06	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
B8h	00									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDx
BAh	01	M 0	MS 00		IR 0	IO 0	T 0	P 01		VCC Power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
BCh	21	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
BEh	B5	Mantissa Exponent								Nom Voltage = 3.0V	Vcc nominal value
C0h	1E	Extension								+0.3V	Extension byte

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
C2h	4D	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
C4h	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
C6h	0A	CISTPL_LINK								Link is 10 bytes	Link to next Tuple
C8h	C1	I 1	D 1	Configuration Index 000001						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDEX
CAh	41	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF
CCh	99	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC power-description structure only P: Power info type T: Timing info present IO: I/O port info present IR: Interrupt info present MS: No memory space M: Misc. info bytes present	TPCE_FS
CEh	01	R 0	DI 0	PI 0	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
D0h	55	X 0	Ah = 5.0				5h = 1V			VCC Nominal is 5 Volts	VCC Nominal Value
D2h	64	R 0	S 1	E 1	IO Add Lines 00100					Supports both 8/16 bit I/O accesses	TPCE_IO
D4h	F0	S 1	P 1	L 1	M 1	V 0	B 0	I 0	N 0	IRQ Sharing Logic Active Pulse & Level mode Interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Bit Mask of IRQ V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Maskable IRQ	TPCE_IR

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
D6h	FF	7 1	6 1	5 1	4 1	3 1	2 1	1 1	0 1	IRQ Levels to be routed 0~7 recommended	TPCE_IR Mask Extension
D8h	FF	F 1	E 1	D 1	C 1	B 1	A 1	9 1	8 1	IRQ Levels to be routed 8~15 recommended	TPCE_IR Mask Extension
DAh	20	X 0	R 0	P 1	RO 0	A 0	Twin 000			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read Only Mode P: Power Down R: Reserved X: More Misc. Fields Byte	TPCE_MI
DCh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
DEh	06	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
E0h	01									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
E2h	01	M 0	MS 00	IR 0	IO 0	T 0	P 01			VCC Power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc info bytes	TPCE_FS
E4h	21	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply vorage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
E6h	B5	Mantissa Exponent								Nom Voltage =3.0V	Vcc nominal value
E8h	1E	Extension								+0.3V	Extension byte
EAh	4D	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
ECh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
EEh	0F	CISTPL_LINK								Link is 16 bytes	Link to next tuple

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
F0h	C2	I 1	D 1	Configuration Index 000010						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDx	
F2h	41	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF	
F4h	99	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info present IO:I/O port info present IR: Interrupt info not present MS: No Mem space M: Misc. info bytes present	TPCE_FS	
F6h	01	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for Vcc	
F8h	55	X 0	Ah = 5.0				5h = 1V			VCC Nominal is 5 Volts	VCC Nominal Value	
FAh	EA	R 1	B 11		I/O 10h					I/O Space Addresses Bus 16/8: Register accesible by 8 or 16 bits I/O: A 1 kbyte I/O address space	TPCE_IO	
FCh	61	L 01		A 10		I/O 01				L: Length 1 byte long A: Address is 4 bytes long		
FEh	F0										1 <sup>st</sup> I/O base address (LSB)	1 <sup>st</sup> I/O range address
100h	01										1 <sup>st</sup> I/O base address (MSB)	
102h	07										1 <sup>st</sup> I/O length - 1	1 <sup>st</sup> I/O range length
104h	F6										2 <sup>nd</sup> I/O base address (LSB)	2 <sup>nd</sup> I/O range length
106h	03										2 <sup>nd</sup> I/O base address (MSB)	
108h	01										2 <sup>nd</sup> I/O length - 1	2 <sup>nd</sup> I/O range length



**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
10Ah	EE	S 1	P 1	L 1	M 0	V 1	B 1	I 1	N 0	IRQ Sharing Logic Active Pulse & Level mode Interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Bit Mask of IRQ V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Maskable IRQ	TPCE_IR
10Ch	20	X 0	R 0	P 1	RO 0	A 0	Twin 001			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc Features	TPCE_MI
10Eh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
110h	06	CISTPL_LINK								Link is 6 bytes	Link to next Tuple
112h	02									Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
114h	01	M 0	MS 00	IR 0	IO 0	T 0	P 01			VCC power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
116h	21	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC
118h	B5	Mantissa Exponent								Nom Voltage = 3.0V	Vcc nominal value
11Ah	1E	Extension								+0.3V	Extension byte

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
11Ch	4D	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
11Eh	1B	CISTPL_CFTABLE_ENTRY								Configuration Entry Tuple	Tuple Code
120h	0F	CISTPL_LINK								Link is 18 bytes	Link to next tuple
122h	C3	I 1	D 1	Configuration Index 000011						I/O Mapped Contiguous D: Default Configuration I: Interface Byte follows	TPCE_INDXX
124h	41	W 0	R 1	P 0	B 0	Interface Type 1				I/O Interface, BVD & WP not used. RDY/BSY# used WAIT# not used	TPCE_IF
126h	99	M 1	MS 00		IR 1	IO 1	T 0	P 01		VCC-Power-description structure only P: Power info type T: Timing info present IO:I/O port info present IR: Interrupt info not present MS: No Mem space M: Misc. info bytes present	TPCE_FS
128h	01	R 0	DI 0	PI 1	AI 0	SI 0	HV 1	LV 1	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for Vcc
12Ah	55	X 0	Ah = 5.0				5h = 1V			Vcc Nominal is 5 Volts	Vcc Nominal Value
12Ch	EA	R 1	B 11		I/O 10h				I/O Space Addresses Bus 16/8: Register accessible by 8 or 16 bits I/O: A 1 kbyte I/O address space	TPCE_IO	
12Eh	61	L 01		A 10		I/O 01				L: Length 1 byte long A: Address is 4 bytes long	
130h	70									1 <sup>st</sup> I/O base address (LSB)	1 <sup>st</sup> I/O range address
132h	01									1 <sup>st</sup> I/O base address (MSB)	
134h	07									1 <sup>st</sup> I/O length - 1	1 <sup>st</sup> I/O range length
136h	76									2 <sup>nd</sup> I/O base address (LSB)	2 <sup>nd</sup> I/O range length

**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function	
138h	03										2 <sup>nd</sup> I/O base address (MSB)	
13Ah	01										2 <sup>nd</sup> I/O length - 1	2 <sup>nd</sup> I/O range length
13Ch	EE	S 1	P 1	L 1	M 0	V 1	B 1	I 1	N 0	IRQ Sharing Logic Active Pulse & Level mode Interrupts supported IREQ 0-15 S: Share Logic Active P: pulse IRQ Supported L: Level IRQ Supported M: Bit Mask of IRQ V: Vendor Specific Signal B: Bus Error signal I: I/O check signal N: Non Maskable IRQ	TPCE_IR	
13Eh	20	X 0	R 0	P 1	RO 0	A 0	Twin 001			Power Down Supported T: Twin Cards Allowed A: Audio Not Supported RO: Read only Mode P: Power-Down Supported R: Reserved X: No More Misc Features	TPCE_MI	
140h	1B	CISTPL_CFTABLE_ENTRY									Configuration Entry Tuple	Tuple Code
142h	06	CISTPL_LINK									Link is 6 bytes	Link to next Tuple
144h	03										Configuration Index Byte No interface configuration byte is present following this byte	TPCE_INDX
146h	01	M 0	MS 00		IR 0	IO 0	T 0	P 01			VCC power-description structure only P: Power info type T: Timing info IO: I/O port info IR: Interrupt info MS: No memory space M: Misc. info bytes	TPCE_FS
148h	21	R 0	DI 0	PI 1	AI 0	SI 0	HV 0	LV 0	NV 1	Nominal operating supply voltage NV: Nominal Voltage LV: Minimum Voltage HV: Maximum Voltage SI: Static Current AI: Average Current PI: Peak Current DI: Power Down Current	Power Parameters for VCC	

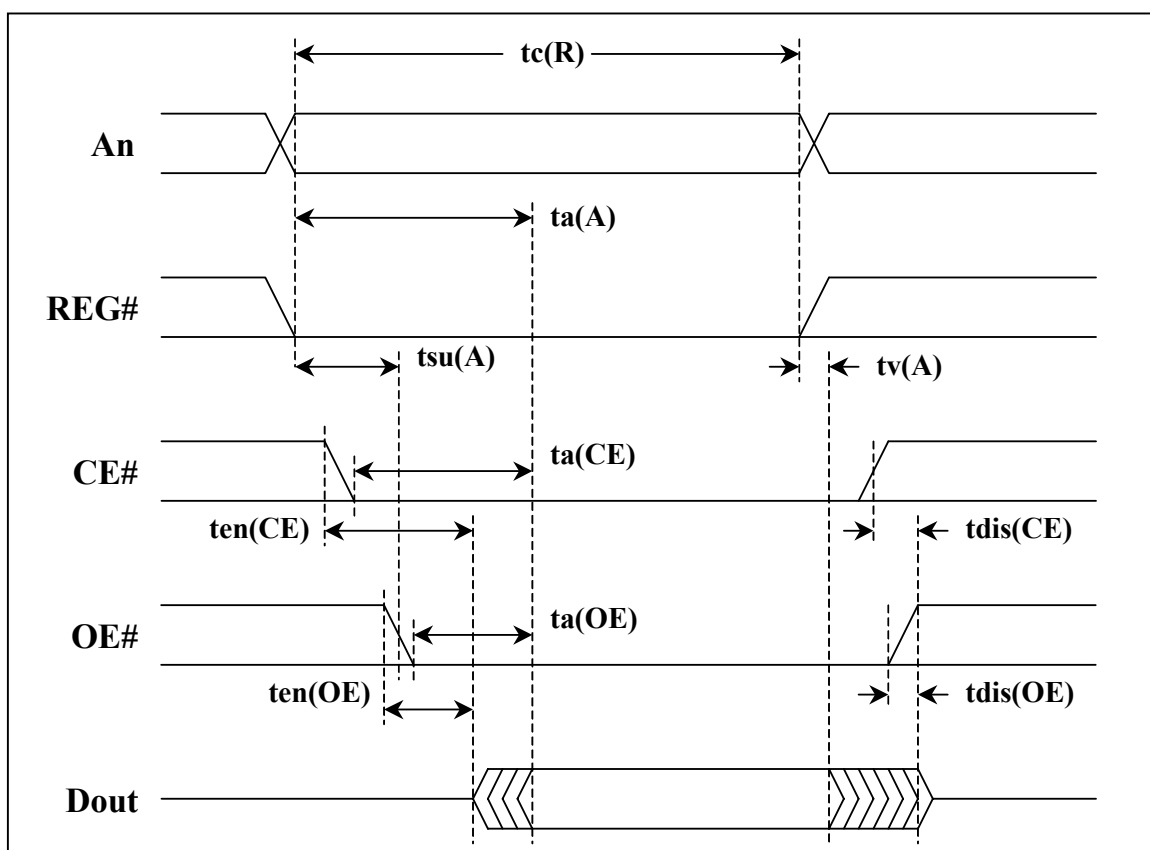
**Card Information Structure (cont)**

Attribute Offset	Data	7	6	5	4	3	2	1	0	Description of Contents	CIS Function
14Ah	B5	Mantissa Exponent								Nom Voltage = 3.0V	Vcc nominal value
14Ch	1E	Extension								+0.3V	Extension byte
14Eh	4D	Mantissa Exponent								Peak I Parameter 2.5mA	Max avg current
150h	14	CISTPL_NO_LINK								No Link Tuple	Tuple Code
152h	00	No Bytes Following								Link is 0 bytes	Link to next Tuple
154h	FF	CISTPL_END								End of list Tuple	Tuple Code

## 6 Timing Information

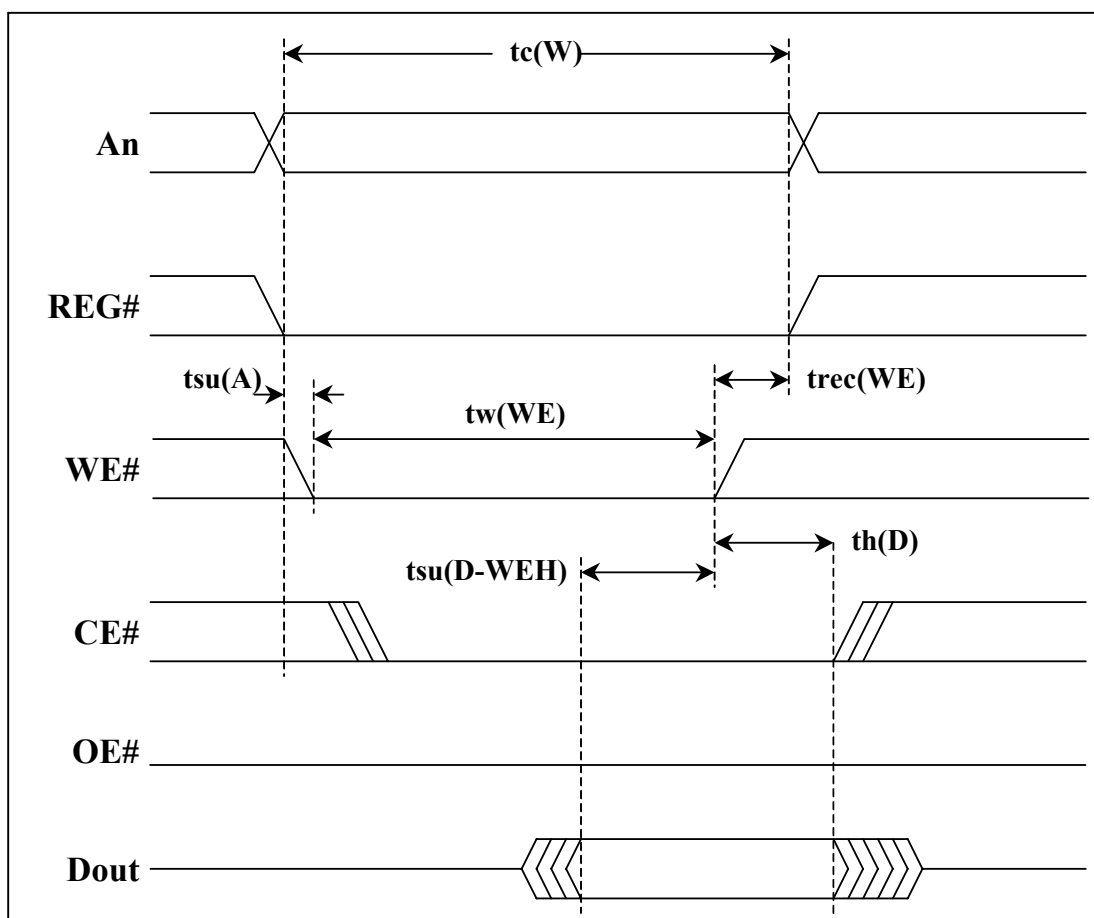
### 6.1.1 Attribute Memory Read Timing

Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Read Cycle Time	tc(R)	tAVAV	300	
Address Access Time	ta(A)	tAVQV		300
Card Enable Access Time	ta(CE)	tELQV		300
Output Enable Access Time	ta(OE)	tGLQV		150
Output Disable Time from CE	tdis(CE)	tEHQZ		100
Output Disable Time from OE	tdis(OE)	tGHQZ		100
Address Setup Time	tsu(A)	tAVWL	30	
Output Enable Time from CE	ten(CE)	tELQNZ	5	
Output Enable Time from OE	ten(OE)	tGLQNZ	5	
Data Valid from Address Change	tv(A)	tAXZX	0	



**6.1.2 Attribute Memory Write Timing**

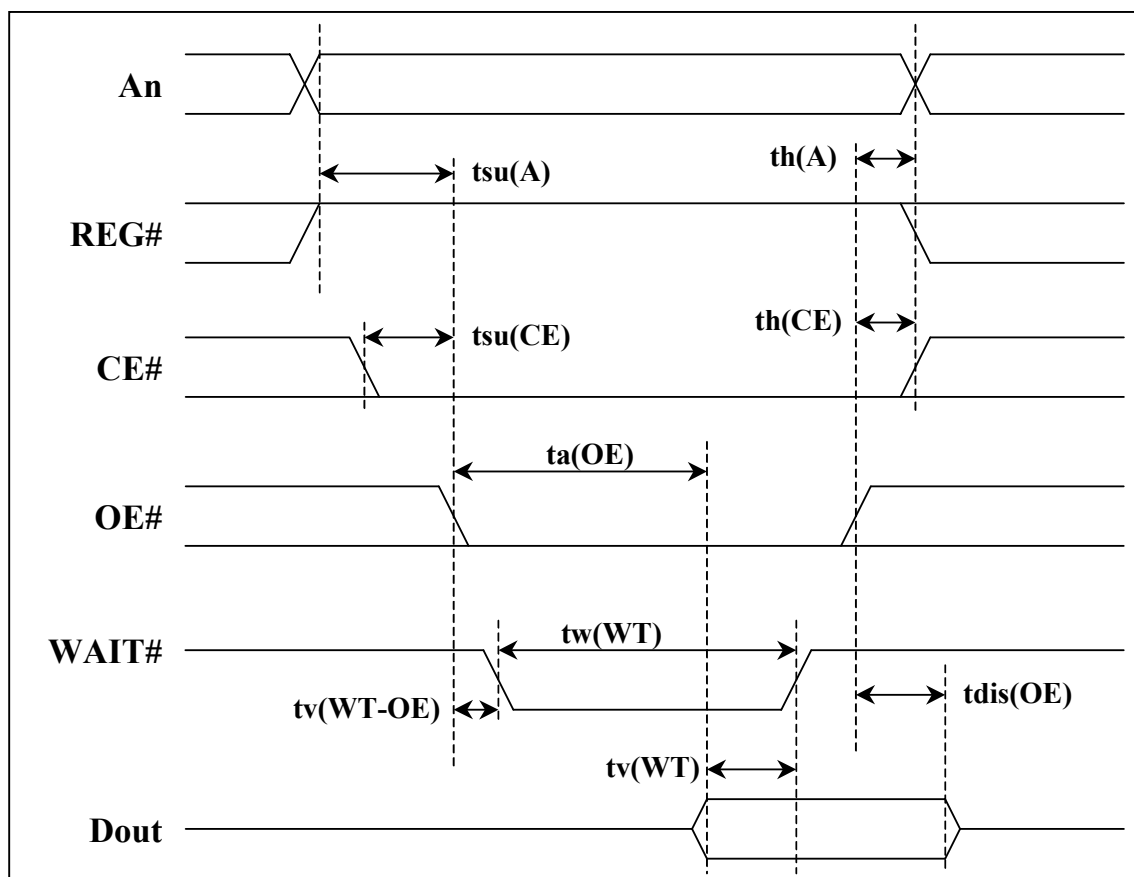
Item	Symbol	IEEE Symbol	Min (ns)	Max (ns)
Write Cycle Time	tc(W)	tAVAV	250	
Write Pulse Width	tw(WE)	tWLWH	150	
Address Setup Time	tsu(A)	tAVWL	30	
Write Recovery Time	trec(WE)	tWMAX	30	
Data Setup Time for WE	tsu(D-WEH)	tDVWH	80	
Data Hold Time	th(D)	tWMDX	30	



**6.1.3 Common Memory Read Timing**

Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Output Enable Access Time	ta(OE)		125		60		50		45
Output Disable Time from OE	t <sub>dis</sub> (OE)		100		60		50		45
Address Setup Time	tsu(A)	30		15		10		10	
Address Hold Time	th(A)	20		15		15		10	
CE Setup before OE	tsu(CE)	0		0		0		0	
CE Hold following OE	th(CE)	20		15		15		10	
Wait Delay Falling from OE	tv(WT-OE)		35		35		35		na <sup>1</sup>
Data Setup for Wait Release	tv(WT)		0		0		0		na <sup>1</sup>
Wait Width Time <sup>2</sup>	tw(WT)		350		350		350		na <sup>1</sup>

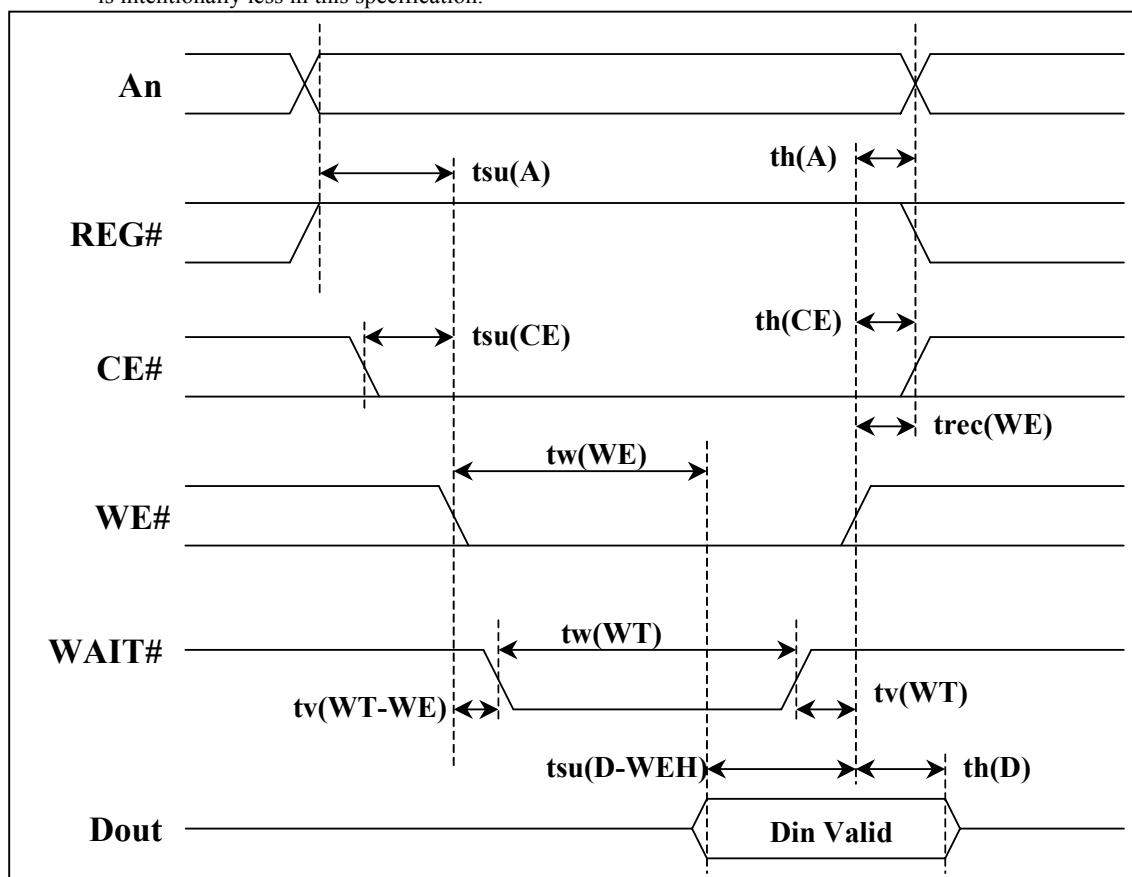
- Notes:
1. WAIT# is not supported in this mode
  2. The WAIT# signal may be ignored if the OE# cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the CIS. The Wait Width time meets PCMCIA specification of 12μs but is intentionally less in this specification.



### 6.1.4 Common Memory Write Timing

Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before WE	tsu(D-WEH)	80		50		40		30	
Data Hold following WE	th(D)	30		15		10		10	
WE Pulse Width	tw(WE)	150		70		60		55	
Address Setup Time	tsu(A)	30		15		10		10	
CE Setup before WE	tsu(CE)	0		0		0		0	
Write Recovery Time	trec(WE)	30		15		15		15	
Address Hold Time	th(A)	20		15		15		15	
CE Hold Following WE	th(CE)	20		15		15		10	
Wait Delay Falling from WE	tv(WT-WE)		35		35		35		na <sup>1</sup>
WE High from Wait Release	tv(WT)	0		0		0		na <sup>1</sup>	
Wait Width Time	tw(WT)		350		350		350		na <sup>1</sup>

- Notes:
1. WAIT# is not supported in this mode
  2. The WAIT# signal may be ignored if the OE# cycle to cycle time is greater than the Wait Width time. The Max Wait Width time can be determined from the CIS. The Wait Width time meets PCMCIA specification of 12μs but is intentionally less in this specification.

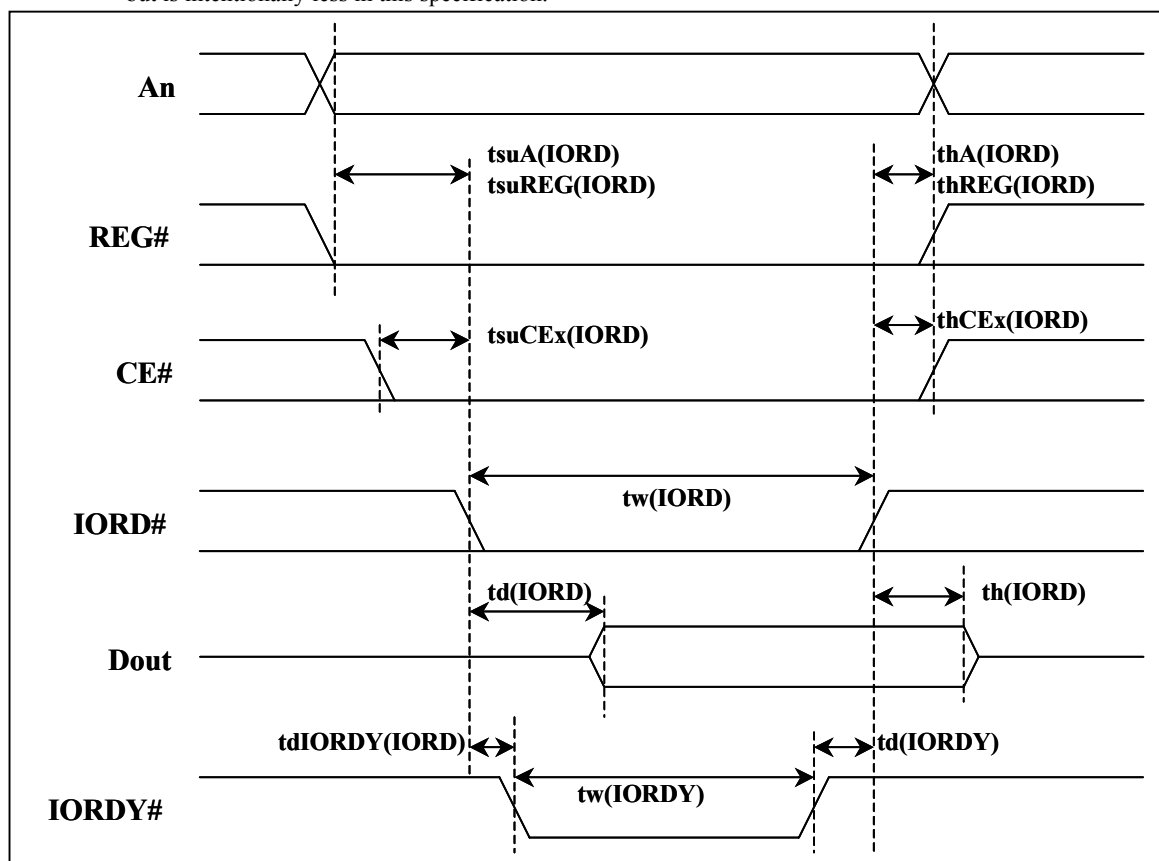




### 6.1.5 I/O Memory Read Timing

Cycle Time Mode:		250 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Delay after IORD	td(IORD)		100		50		50		45
Data Hold following IORD	th(IORD)	0		5		5		5	
IORD Width Time	tw(IORD)	165		70		65		55	
Address Setup before IORD	tsuA(IORD)	70		25		25		15	
Address Hold following IORD	thA(IORD)	20		10		10		10	
CE Setup before IORD	tsuCE(IORD)	5		5		5		5	
CE Hold following IORD	thCE(IORD)	20		10		10		10	
REG Setup before IORD	tsuREG(IORD)	5		5		5		5	
REG Hold following IORD	thREG(IORD)	0		0		0		0	
Wait Delay Falling from IORD <sup>2</sup>	tdIORDY(IORD)		35		35		35		na <sup>1</sup>
Data Delay from Wait Rising <sup>2</sup>	td(IORDY)		0		0		0		na <sup>1</sup>
Wait Width Time <sup>2</sup>	tw(IORDY)		350		350		350		na <sup>1</sup>

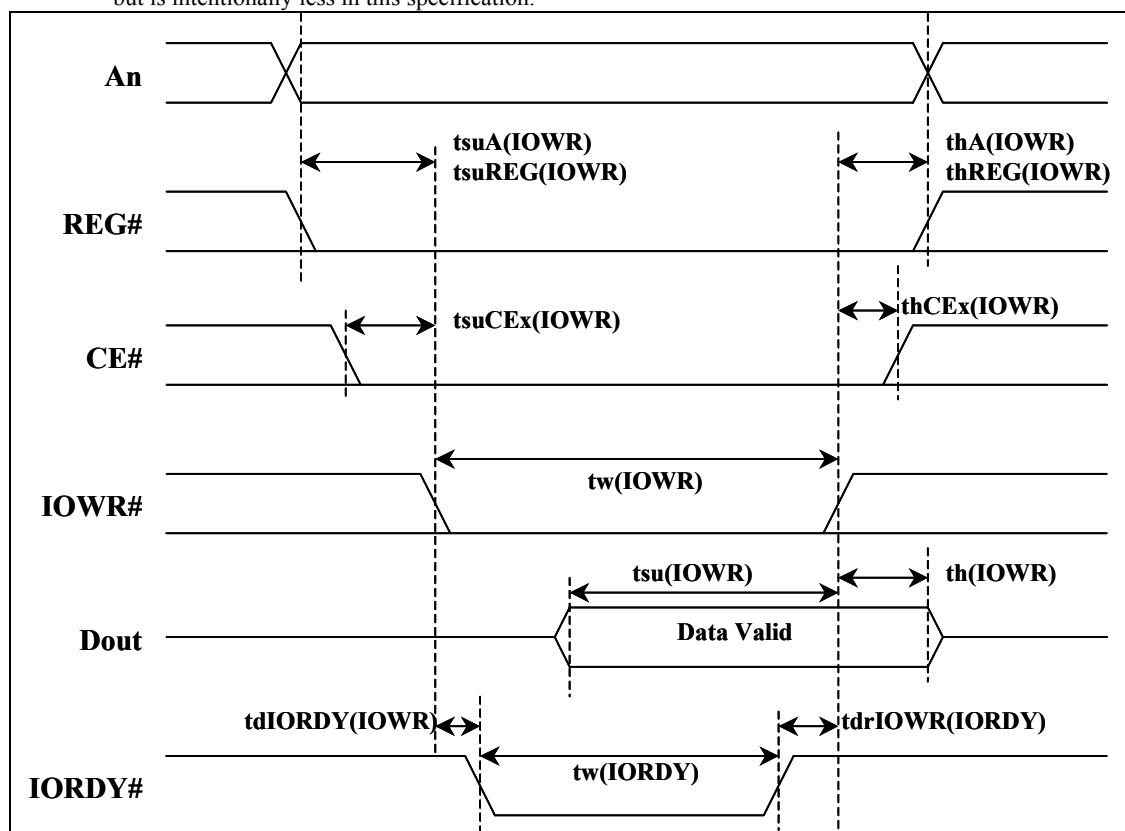
- Notes:
1. IORDY is not supported in this mode
  2. Minimum time from IORDY high to IORD high is 0msec, but minimum IORD width shall still be met. HD signifies data provided by the ATA Card to the system. The Wait Width time meets PCMCIA specification of 12μs but is intentionally less in this specification.



### 6.1.6 I/O Memory Write Timing

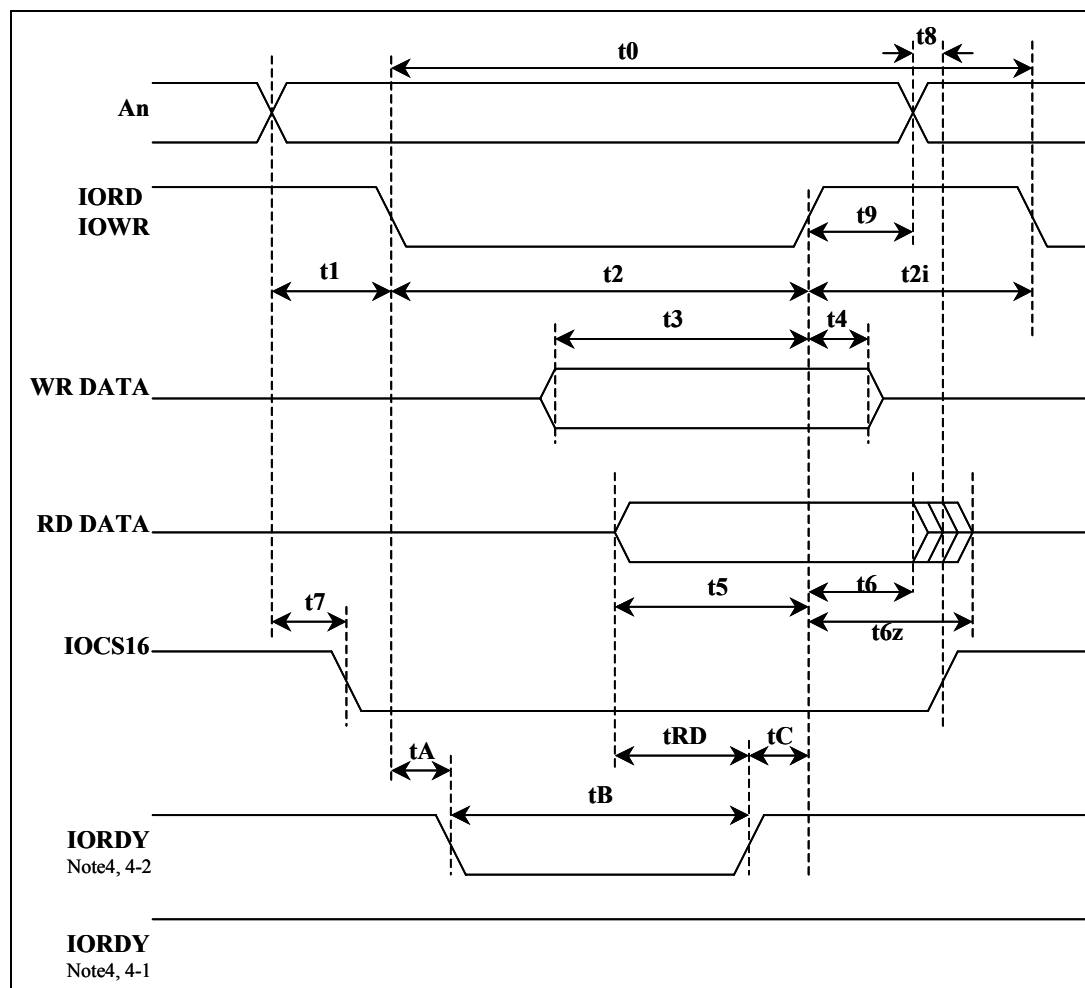
Cycle Time Mode:		255 ns		120 ns		100 ns		80 ns	
Item	Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Data Setup before IOWR	tsu(IOWR)	60		20		20		15	
Data Hold following IOWR	th(IOWR)	30		10		5		5	
IOWR Width Time	tw(IOWR)	165		70		65		55	
Address Setup before IOWR	tsuHA(IOWR)	70		25		25		15	
Address Hold following IOWR	thHA(IOWR)	20		20		10		10	
CEx Setup before IOWR	tsuCEX(IOWR)	5		5		5		5	
CEx Hold following IOWR	thCEX(IOWR)	20		20		10		10	
REG# Setup before IOWR	tsuREG(IOWR)	5		5		5		5	
REG# Hold before IOWR	thREG(IOWR)	0		0		0		0	
Wait Delay Falling from IOWR <sup>2</sup>	tdIORDY(IOWR)		35		35		35		na <sup>1</sup>
IOWR high from Wait high <sup>2</sup>	tdrIOWR(IORDY)	0		0		0		na <sup>1</sup>	
Wait Width Time <sup>2</sup>	Tw(IORDY)		350		350		350		na <sup>1</sup>

- Notes:
1. IORDY is not supported in this mode
  2. Minimum time from IORDY high to IORD high is 0msec, but minimum IORD width shall still be met. HD signifies data provided by the ATA Card to the system. The Wait Width time meets PCMCIA specification of 12μs but is intentionally less in this specification.



**6.1.7 True IDE Mode Read/Write Timing**

	Item	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 6
t0	Cycle Time (min)	600	383	240	180	120	100	80
t1	Address Valid to HIOE/HIOW setup (min)	70	50	30	30	25	15	10
t2	IORD#/IOWR# (min)	165	125	100	80	70	65	55
t2	IORD#/IOWR# (min) Register (8 bit)	290	290	290	80	70	65	55
t2i	IORD#/IOWR#recovery time (min)	-	-	-	70	25	25	20
t3	IOWR# data setup (min)	60	45	30	30	20	20	15
t4	IOWR# data hold (min)	30	20	15	10	10	5	5
t5	IORD# data setup (min)	50	35	20	20	20	15	10
t6	IORD# data hold (min)	5	5	5	5	5	5	5
t6Z	IORD# data tristate (max)	30	30	30	30	30	20	20
t7	Address valid to IOCS16 assertion (max)	90	50	40	n/a	n/a	n/a	n/a
t8	Address valid to IOCS16 released (max)	60	45	30	n/a	n/a	n/a	n/a
t9	IORD#/IOWR#to address valid hold	20	15	10	10	10	10	10
tRD	Read Data Valid to IORDY active (min) If IORDY initially low after tA	0	0	0	0	0	0	0
tA	IORDY Setup Time	35	35	35	35	35	na	na
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	na	na
tC	IORDY assertion to release (max)	5	5	5	5	5	na	na

**True IDE Mode Read/Write timing (cont)**

**True IDE Mode Read/Write Timing Diagram**

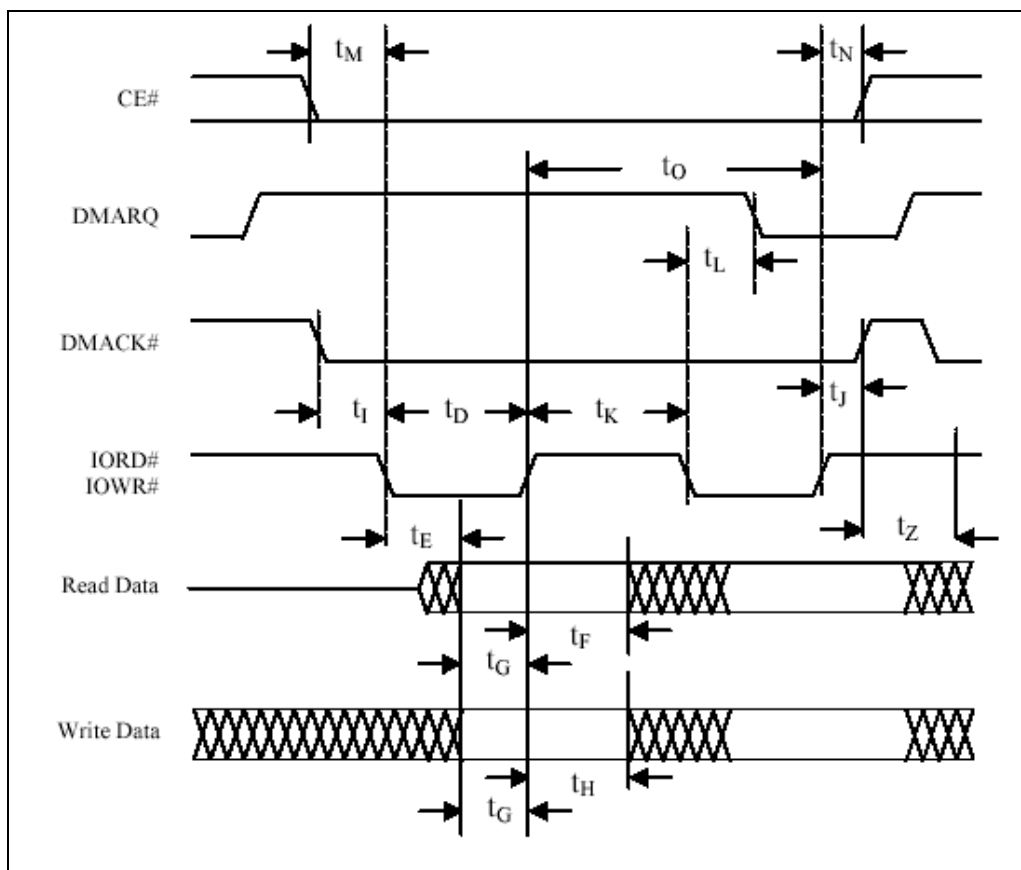
- Notes:
1. Device address consists of CE0, CE1, and A[2:0]
  2. Data consists of D[15:0] (16-bit) or D[7:0] (8-bit)
  3. IOCS16 is shown for PIO modes 0, 1, and 2. For other modes, this signal is ignored.
  4. The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after  $t_A$  from the assertion of IORD or IOWR. The assertion and negation of IORDY is described in the following three cases.
    - 4-1. Device never negates IORDY: No wait is generated
    - 4-2. Device drives IORDY low before  $t_A$ : wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and IORD is asserted, the device shall place read data on D15:0 for  $t_{RD}$  before causing IORDY to be asserted.

**6.1.8 True IDE Multiword DMA Mode Read/Write Timing**

	Item	Mode 0 (ns)	Mode 1 (ns)	Mode 2 (ns)	Mode 3 (ns)	Mode 4 (ns)
t <sub>O</sub>	Cycle time (min) <sup>1</sup>	480	150	120	100	80
t <sub>D</sub>	IORD# / IOWR# asserted width (min) <sup>1</sup>	215	80	70	65	55
t <sub>E</sub>	IORD# data access (max)	150	60	50	50	45
t <sub>F</sub>	IORD# data hold (min)	5	5	5	5	5
t <sub>G</sub>	IORD# / IOWR# data setup (min)	100	30	20	15	10
t <sub>H</sub>	IOWR# data hold (min)	20	15	10	5	5
t <sub>I</sub>	DMACK# to IORD# / IOWR# setup	0	0	0	0	0
t <sub>J</sub>	IORD# / IOWR# to -DMACK hold (min) <sup>1</sup>	20	5	5	5	5
t <sub>KR</sub>	IORD# negated width (min) <sup>1</sup>	50	50	25	25	20
t <sub>KW</sub>	IOWR# negated width (min)	215	50	25	25	20
t <sub>LR</sub>	IORD# to DMARQ delay (max)	120	40	35	35	35
t <sub>LW</sub>	IOWR# to DMARQ delay (Max)	40	40	35	35	35
t <sub>M</sub>	CEx valid to IORD# / IOWR#	50	30	25	10	5
t <sub>N</sub>	CEx hold	15	10	10	10	10
t <sub>Z</sub>	DMACK#	20	25	25	25	25

**Notes:**

1) t<sub>O</sub> is the minimum total cycle time and t<sub>D</sub> is the minimum command active time, while t<sub>KR</sub> and t<sub>KW</sub> are the minimum command recovery time or command inactive time for input and output cycles respectively. The actual cycle time equals the sum of the actual command inactive time. The three timing requirements t<sub>O</sub>, t<sub>D</sub>, t<sub>KR</sub>, and t<sub>KW</sub> shall be met. The minimum total cycle time requirement is greater than the sum of t<sub>D</sub> and t<sub>KR</sub> or t<sub>KW</sub> for input and output cycles respectively. This means a host implementation can lengthen either or both of t<sub>D</sub> and either of t<sub>KR</sub>, and t<sub>KW</sub> as needed to ensure that t<sub>O</sub> is equal to or greater than the value reported in the device's identify device data. An ATA Flash Card implementation shall support any legal host implementation.

**True IDE Mode Multiword DMA Read/Write timing (cont)**

**Notes:**

- 1) If the Card cannot sustain continuous, minimum cycle time DMA transfers, it may negate DMARQ within the time specified from the start of the DMA transfers in progress and reassert the signal at a later time to continue the DMA operation.
- 2) DMACK# may be negated by the host to suspend the DMA transfer in progress.

## 7 Electrical Characteristics

### 7.1 Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V <sub>CC</sub>	Input Power	-0.3 ~ 6.0	V
T <sub>STG</sub>	Storage Temperature	-65 ~ 150	°C
I <sub>OP</sub>	Operating Current	50	mA
		60	mA
I <sub>STB</sub>	Standby Current	1.5	mA
		2	mA

### 7.2 Recommended Operating Conditions

Symbol	Parameter		Ratings	Unit
V <sub>CC</sub>	Input Power	5V	4.5 to 5.5	V
		3.3V	3.13 to 3.47	V
T <sub>A</sub>	Operating Temperature	Commercial	0 to 70	°C
		Industrial	-40 to 85	°C

**7.3 DC Electrical Characteristics**

 (T<sub>A</sub> = 0 to 70°C V<sub>DD</sub> = 3.3V +/-5%)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	High Level Input Voltage	CMOS		2.4			V
V <sub>IL</sub>	Low Level Input Voltage	CMOS				0.6	V
V <sub>T</sub>	Switching Threshold	CMOS			1.8		V
V <sub>T+</sub>	Switching Threshold, Positive Going Threshold	CMOS				2.0	V
V <sub>T-</sub>	Switching Threshold, Negative Going Threshold	CMOS		1.0			V
I <sub>IH</sub>	High Level Input Current	Input Buffer	V <sub>IN</sub> = V <sub>DD</sub>	-10		10	uA
		Input Buffer with pull-up		-160	-30	-10	uA
I <sub>IL</sub>	Low Level Input Current	Input Buffer	V <sub>IN</sub> = V <sub>SS</sub>	-10		10	uA
		Input Buffer with pull-up		-160	-30	-10	uA
V <sub>OH</sub>	High Level Output Current			2.4			V
V <sub>OL</sub>	Low Level Output Current					0.4	V
I <sub>OZ</sub>	Tri-state Leakage Current		V <sub>OUT</sub> = V <sub>SS</sub> or V <sub>DD</sub>	-10		10	uA
I <sub>DD</sub>	Maximum Operating Current		V <sub>DD</sub> = 3.0V F <sub>CLK</sub> = 20MHz		30	40	mA
I <sub>idle</sub>	Idle Current					20	mA
I <sub>ds</sub>	Stop Current					30	uA



**DC Electrical Characteristics (cont.)**

(TA = 0 to 70°C VDD = 5V +/-10%)

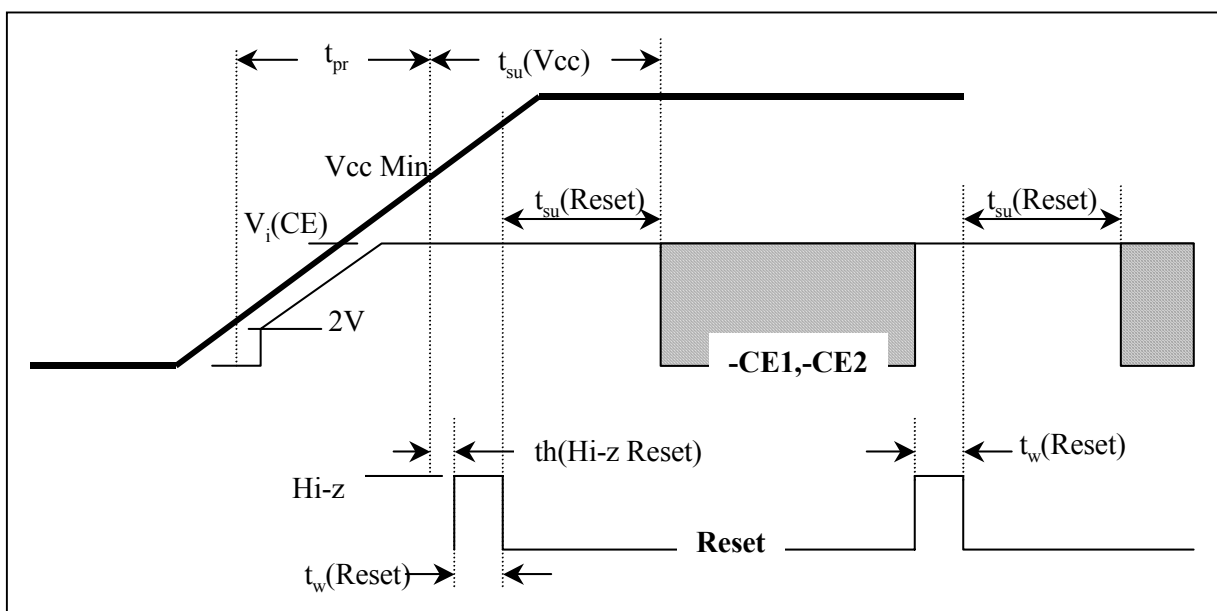
Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	High Level Input Voltage	CMOS		3.5			V
		TTL		2.0			V
V <sub>IL</sub>	Low Level Input Voltage	CMOS				1.5	V
		TTL				0.8	V
V <sub>T</sub>	Switching Threshold	CMOS			2.5		V
		TTL			1.4		V
V <sub>T+</sub>	Switching Threshold, Positive Going Threshold	CMOS				4.0	V
		TTL				2.0	V
V <sub>T-</sub>	Switching Threshold, Negative Going Threshold	CMOS		1.0			V
		TTL		0.8			V
I <sub>IH</sub>	High Level Input Current	Input Buffer	V <sub>IN</sub> = V <sub>DD</sub>	-10		10	uA
		Input Buffer with pull-up		10	50	100	uA
I <sub>IL</sub>	Low Level Input Current	Input Buffer	V <sub>IN</sub> = V <sub>SS</sub>	-10		10	uA
		Input Buffer with pull-up		-100	-50	-10	uA
V <sub>OH</sub>	High Level Output Current			2.4			V
V <sub>OL</sub>	Low Level Output Current					0.4	V
I <sub>OZ</sub>	Tri-state Leakage Current		V <sub>OUT</sub> = V <sub>SS</sub> or V <sub>DD</sub>	-10		10	uA
I <sub>DD</sub>	Maximum Operating Current		V <sub>DD</sub> = 303V		60	70	mA
I <sub>idle</sub>	Idle Current		F <sub>CLK</sub> = 20MHz			35	mA
I <sub>ds</sub>	Stop Current					60	uA

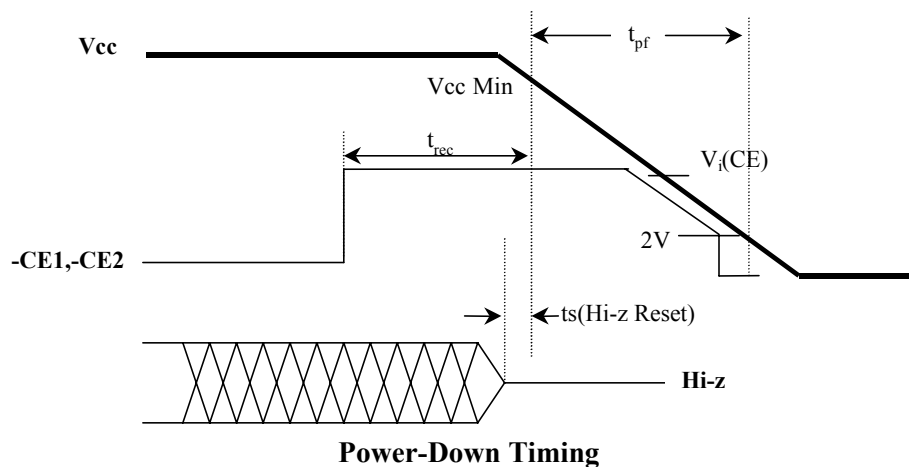
### 7.4 Power-up/Power-down Timing

The following timing requirements are defined to permit the ATA controller to perform power-up initialization and to complete procedures prior to power down.

Item	Symbol	Condition	Value		
			Min	Max	Unit
Card Enable Signal Level <sup>1</sup>	Vi(CE)	$0V \leq V_{cc} < 2.0V$	0	ViMAX	V
		$2.0V \leq V_{cc} < V_{IH}$	$V_{cc}-0.1$	ViMAX	V
		$V_{IH} \leq V_{cc}$	$V_{IH}$	ViMAX	V
Card Enable Setup Time	$t_{su}(V_{cc})$		20		ms
RESET Setup Time	$t_{su}(\text{RESET})$		20		ms
Card Enable Recover Time	$t_{rec}(V_{cc})$		0.001		ms
Vcc Rising Time	$t_{pr}$	$10\% \rightarrow 90\%$ of Vcc	0.1	100	ms
Vcc Falling Time	$t_{pf}$	$90\%$ of Vcc $\rightarrow 10\%$	3.0	300	ms
RESET Width	$t_w(\text{RESET})$		10		us
	$t_h(\text{Hi-z RESET})$		1		ms
	$t_s(\text{Hi-z RESET})$		0		ms

1. ViMAX means Absolute Maximum Voltage for Input in the period of  $0V \leq V_{cc} < 2.0V$ , Vi(CE) is only  $0V \sim ViMAX$
2. The  $t_{pr}$  and  $t_{pf}$  are defined as “linear waveform” in the period of 10% to 90% or vice-versa. Even if the waveform is not “linear waveform”, its rising and falling time must be met by this specification.



**Power-Up / Power-Down Timing (cont.)**


**Disclaimer:**

No part of this document may be copied or reproduced in any form or by any means, or transferred to any third party, without the prior written consent of an authorized representative of SMART Modular Technologies, Inc. ("SMART"). The information in this document is subject to change without notice. SMART assumes no responsibility for any errors or omissions that may appear in this document, and disclaims responsibility for any consequences resulting from the use of the information set forth herein. SMART makes no commitments to update or to keep current information contained in this document. The products listed in this document are not suitable for use in applications such as, but not limited to, aircraft control systems, aerospace equipment, submarine cables, nuclear reactor control systems and life support systems. Moreover, SMART does not recommend or approve the use of any of its products in life support devices or systems or in any application where failure could result in injury or death. If a customer wishes to use SMART products in applications not intended by SMART, said customer must contact an authorized SMART representative to determine SMART's willingness to support a given application. The information set forth in this document does not convey any license under the copyrights, patent rights, trademarks or other intellectual property rights claimed and owned by SMART. The information set forth in this document is considered to be "Proprietary" and "Confidential" property owned by SMART.

ALL PRODUCTS SOLD BY SMART ARE COVERED BY THE PROVISIONS APPEARING IN SMART'S TERMS AND CONDITIONS OF SALE ONLY, INCLUDING THE LIMITATIONS OF LIABILITY, WARRANTY AND INFRINGEMENT PROVISIONS. SMART MAKES NO WARRANTIES OF ANY KIND, EXPRESS, STATUTORY, IMPLIED OR OTHERWISE, REGARDING INFORMATION SET FORTH HEREIN OR REGARDING THE FREEDOM OF THE DESCRIBED PRODUCTS FROM INTELLECTUAL PROPERTY INFRINGEMENT, AND EXPRESSLY DISCLAIMS ANY SUCH WARRANTIES INCLUDING WITHOUT LIMITATION ANY EXPRESS, STATUTORY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

©2005 SMART Modular Technologies, Inc. All rights reserved.