

PXI-2000 Series

4-CH, 14/16-Bit, Up to 2MS/s Simultaneous-Sampling Multi-Function PXI Modules

Features

- PXI specifications Rev. 2.0 compliant
- 3U Eurocard form factor, CompactPCI compliant (PICMG 2.0 R3.0)
- 4-CH differential analog inputs
- Up to 2 MS/s simultaneous-sampling rate (PXI-2010)
- 14-bit A/D resolution (PXI-2010)
- 16-bit A/D resolution (PXI-2005 and PXI-2006)
- On-board 8k-sample A/D FIFO (PXI-2010)
- Bipolar or unipolar analog input ranges
- Programmable gains of x1, x2, x4, x8
- Scatter-gather DMA for both analog inputs and outputs
- 2-CH 12-bit multiplying analog outputs with waveform generation
- On-board 2k-sample D/A FIFO
- 24-CH TTL digital input/output
- 2-CH 16-bit general purpose timer/counter
- Analog and digital triggering
- Fully auto calibration
- Multiple modules synchronization through PXI trigger bus

Operating Systems

- Windows 2000/NT/XP/98
- Red Hat Linux
- Windows CE (call for availability)

Recommended Software

- VB/VC++/BCB/Delphi
- DAQBench

Driver Support

- D2K-DASK:
 - Windows 2000/NT/XP/98 driver
- D2K-DASK/X: Red Hat Linux driver
- D2K-LVIEW: LabVIEW driver
- D2K-MTLB: MATLAB driver
- D2K-OCX: 32-bit ActiveX controls



Introduction

ADLINK PXI-2010, PXI-2005, and PXI-2006 are simultaneous-sampling multifunction PXI modules to meet a wide range of application requirements. These products can simultaneously sample 4 AI channels with differential input configurations to achieve maximum noise elimination. They also provide 2-CH 12-bit analog outputs with waveform generation capabilities, which can be performed together with analog input functions. If more analog input or output channels are required, multiple modules can be synchronized through the PXI trigger bus. This makes the PXI-2000 series ideal for stimulus/response tests.

The PXI-2000 series also feature analog and digital triggering, 24-CH programmable digital I/O lines, and 2-CH 16-bit general-purpose timer/counters. The auto-calibration feature adjusts the gain and offset to a specified accuracy, eliminating the need to calibrate the modules by adjusting trimpots.

Termination Boards

DIN-68S/1M

Termination Board with a 68-pin SCSI-II Connector and DIN-Rail Mounting (Including One 1-meter ACL-10568 Cable)



Termination board DIN-68S/1M

Ordering Information

- **PXI-2010**
4-CH 14-Bit 2 MS/s Simultaneous-Sampling Multi-Function PXI Module
- **PXI-2005**
4-CH 16-Bit 500 kS/s Simultaneous-Sampling Multi-Function PXI Module
- **PXI-2006**
4-CH 16-Bit 250 kS/s Simultaneous-Sampling Multi-Function PXI Module

Pin Assignment

Connector Pin Assignment

CH0+	1	35	CH0-
CH1+	2	36	CH1-
CH2+	3	37	CH2-
CH3+	4	38	CH3-
EXTATRIG	5	39	AIGND
DA1OUT	6	40	AOGND
DA0OUT	7	41	AOGND
AOEXTREF	8	42	AOGND
SDI3_1 / NC*	9	43	SDI3_0 / NC*
SDI2_1 / NC*	10	44	SDI2_0 / NC*
SDI1_1 / NC*	11	45	SDI1_0 / NC*
SDI0_1 / NC*	12	46	SDI0_0 / NC*
AO_TRIG_OUT	13	47	EXTWFTRG
AI_TRIG_OUT	14	48	EXTDTRIG
GPTC1_SRC	15	49	DGND
GPTC0_SRC	16	50	DGND
GPTC0_GATE	17	51	GPTC1_GATE
GPTC0_OUT	18	52	GPTC1_OUT
GPTC0_UPDOWN	19	53	GPTC1_UPDOWN
EXTTIMEBASE	20	54	DGND
AF11	21	55	AF10
PB7	22	56	PB6
PB5	23	57	PB4
PB3	24	58	PB2
PB1	25	59	PB0
PC7	26	60	PC6
PC5	27	61	PC4
DGND	28	62	DGND
PC3	29	63	PC2
PC1	30	64	PC0
PA7	31	65	PA6
PA5	32	66	PA4
PA3	33	67	PA2
PA1	34	68	PA0

*Pin 9~12 and pin 43~46 are SDI<0..3>_n for PXI-2010 ; NC for PXI-2005 and PXI-2006

Quick Selection Guide

Model number	Analog Input				Analog Output			DIO	Timer/Counter
	No. of channels	Resolution	Sampling rate	Input range	No. of channels	Resolution	Update rate	No. of channels	No. of channels
PXI-2010	4-CH DI	14 bits	2 MS/s	±1.25 V to ±10 V	2	12 bits	1 MS/s	24-CH 8255 PIO	2-CH, 16-bit
PXI-2005	4-CH DI	16 bits	500 kS/s	±1.25 V to ±10 V	2	12 bits	1 MS/s	24-CH 8255 PIO	2-CH, 16-bit
PXI-2006	4-CH DI	16 bits	250 kS/s	±1.25 V to ±10 V	2	12 bits	1 MS/s	24-CH 8255 PIO	2-CH, 16-bit

Specifications

Model Number	PXI-2010	PXI-2005	PXI-2006
Analog Input			
Resolution	14 bits, no missing codes	16 bits, no missing codes	16 bits, no missing codes
Number of channels	4 simultaneous-sampling channels with differential input		
Maximum sampling rate	2 MS/s	500 kS/s	250 kS/s
Programmable gain	1,2,4,8		
Bipolar input ranges	±10 V, ±5 V, ±2.5 V, ±1.25 V		
Unipolar input ranges	0-10 V, 0-5 V, 0-2.5 V, 0-1.25 V		
Offset error	±3 mV	±1 mV	±1 mV
Gain error	±0.03% of FSR	±0.01% of FSR	±0.01% of FSR
Input Coupling	DC		
Overvoltage protection	Power on: continuous ±35 V, power off: continuous ±15 V		
Input Impedance	1 GΩ/100 pF		
CMRR (gain = 1)	85 dB		
-3dB small signal bandwidth (gain = 1)	1 MHz	700 kHz	400 kHz
Trigger sources	Software, external digital/analog trigger, PXI trigger bus		
Trigger modes	Pre-trigger, post-trigger, middle-trigger, delay-trigger, and repeated trigger		
FIFO buffer size	8 k samples	512 samples	512 samples
Data Transfers	Polling, scatter-gather DMA		
Analog Output			
Number of channels	2 voltage outputs		
Resolution	12 bits		
Output ranges	0-10 V, ±10 V, 0-AOEXTREF, ±AOEXTREF		
Maximum update rate	1 μs		
Slew rate	20 V/μs		
Settling time	3 μs to ±0.5 LSB accuracy		
Offset error	±1 mV		
Gain error	±0.02% of max. output		
Driving capacity	±5 mA		
Stability	Any passive load, up to 1500 pF		
Trigger sources	Software, external digital/analog trigger, PXI trigger bus		
Trigger modes	Post-trigger, delay-trigger, and repeated trigger		
FIFO buffer size	2 k samples		
Data transfers	Programmed I/O, scatter-gather DMA		
Digital I/O			
Number of channels	24-CH 8255 programmable input/output		
Compatibility	5 V/TTL		
Data transfers	Programmed I/O		
Timer/Counter			
Number of channels	2		
Resolution	16 bits		
Compatibility	5 V/TTL		
Base clock available	40 MHz, external clock up to 10 MHz		
Auto Calibration			
On-board reference	+5 V		
Temperature drift	±2 ppm/°C		
Stability	±6 ppm/1000 Hrs		
General Specifications			
Dimensions	160 mm x 100 mm (not including connectors)		
Connector	68-pin VHDCI female		
Operating temperature	0 to 55 °C		
Storage temperature	-20 to 80 °C		
Humidity	5 to 95%, noncondensing		
Power requirement	+5 V 1.82 A typical	+5 V 2.04 A typical	+5 V 1.82 A typical

* All specifications are subject to change without further notice.

