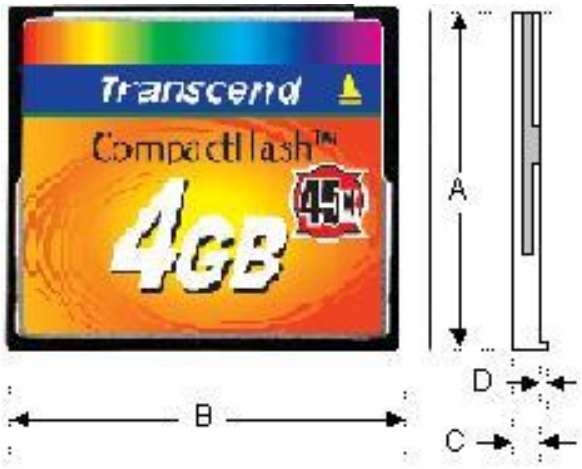
TS4GCF45

4GB CompactFlash Card

Description

The TS4GCF45 is a 4GB CompactFlash Card with 4 pcs of 1Gx8 Flash Memory assembled on printed circuit board.

Placement



Features

- Storage Capacity: 4GB
- Single Power Supply: 5V ± 10% or 3.3V ± 10%
- Operating Temperature: 0°C to 70°C
- Host Interface: 8/16-bit access

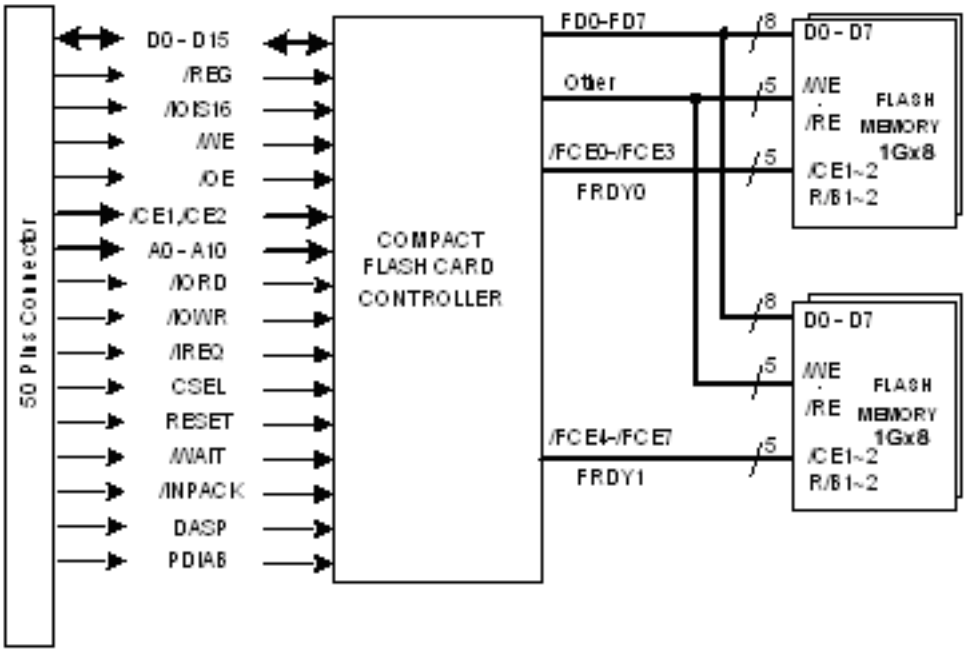
  Flash Interface: 8-bit access
- Endurance: 100,000 Program/Erase cycles
- Durability of Connector: 10,000 times

Dimensions

Side	Millimeters	Inches
A	36.40 ± 0.150	1.43 ± 0.005
B	42.80 ± 0.100	1.69 ± 0.004
C	3.30 ± 0.100	0.13 ± 0.004
D	0.63 ± 0.070	0.02 ± 0.003

Block Diagram

- **With 4 pcs of 1Gx8 Flash Memory**



Pinouts

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
01	VSS	14	A6	27	D11	40	NC
02	D3	15	A5	28	D12	41	RESET
03	D4	16	A4	29	D13	42	/WAIT
04	D5	17	A3	30	D14	43	/INPACK
05	D6	18	A2	31	D15	44	/REG
06	D7	19	A1	32	/CE2	45	DASP
07	/CE1	20	A0	33	VSS	46	PDIAG
08	A10	21	D0	34	/IORD	47	D8
09	/OE	22	D1	35	/IOWR	48	D9
10	A9	23	D2	36	/WE	49	D10
11	A8	24	/IOIS16	37	/IREQ	50	VSS
12	A7	25	VSS	38	VCC		
13	VCC	26	VSS	39	CSEL		

Pin Identification

Symbol	Function
D0 ~ D15	Data Bus (Bi-directional)
A0 ~ A10	Address Bus (Input)
/CE1,/CE2	Card Enable (Input)
/OE, /WE	Output / Write Enable (Input)
/REG	Register Select (Input)
/IORD, /IOWR	I/O Access (Input)
/IREQ, /IOIS16, RESET, CSEL, /INPACK, /WAIT, DASP, PDIAG	I/O Handshaking (Input/Output)
VSS	Ground
VCC	Vcc Power Input

CompactFlash I/O Mapping Address

PTnREG	Primary I/O PIHA[10:0]	Secondary I/O PIHA[10:0]	Independent I/O PIHA[3:0]	PInIORD = L	PInIOWR = L
L	1F0H	170H	0H	Read Even Data	Write Even Data
L	1F1H	171H	1H	Error Register	Feature Register
L	1F2H	172H	2H	Sector Count	Sector Count
L	1F3H	173H	3H	Sector Number	Sector Number
L	1F4H	174H	4H	Cylinder Low	Cylinder Low
L	1F5H	175H	5H	Cylinder High	Cylinder High
L	1F6H	176H	6H	Drive/Head	Drive/Head
L	1F7H	177H	7H	Status Register	Command
L	---	---	8H	Duplicate Read Even Data	Duplicate Write Even Data
L	---	---	9H	Duplicate Read Odd Data	Duplicate Write Odd Data
L	---	---	0DH	Duplicate Error	Duplicate Feature
L	3F6H	376H	0EH	Alternate Status	Device Control
L	3F7H	377H	0FH	Drive Address	Reserved

Absolute Maximum Rating

Parameter	Symbol	Min	Max	Unit
DC Power Supply	VDD-VSS	-0.6	+6	V
Power Supply Voltage	V_{CC}	-0.3	3.6	V
Operating Temperature	Ta	0	+70	°C
Storage Temperature	Tst	-55	+150	°C

DC Characteristics (Ta = 0°C to 70°C, Vcc = 3.3V ±10%)

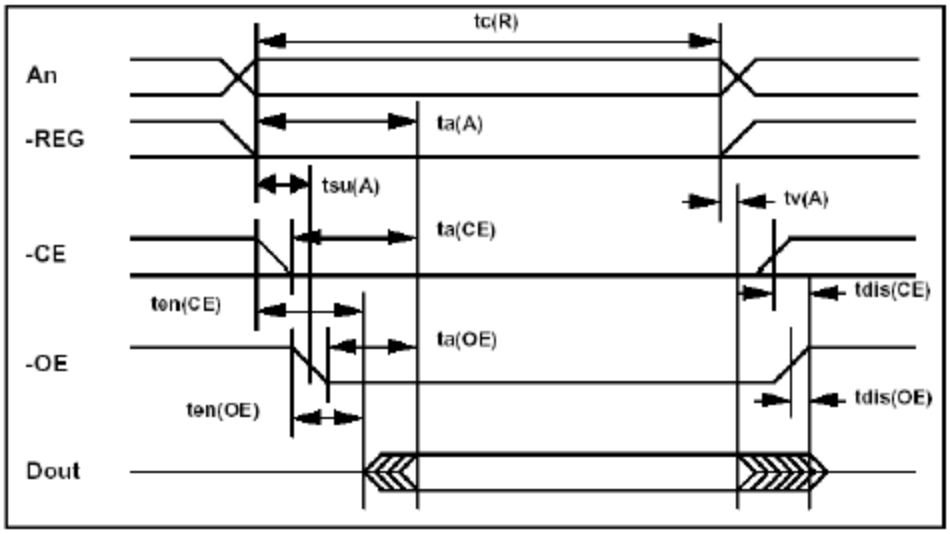
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	VIH	--	2.3	--	--	V
	VIL	--	--	--	0.2 x Vcc	V
Output Voltage	VOH	IOL = 4,8mA	Vcc – 0.8	--	--	V
	VOL	IOL = 4,8mA	--	--	0.4	V
Input Leakage Current	ILK	VIH = VDD / VIL = GND	-1	--	1	uA
Sleep Current	ISP	--	--	0.5	1	mA
Sector Read Current	ISR	--	--	17	22	mA
Sector Write Current	ISW	--	--	22	28	mA

DC Characteristics (Ta = 0°C to 70°C, Vcc = 5.0V ±10%)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage	VIH	--	2.0	--	--	V
	VIL	--	--	--	0.2 x Vcc	V
Output Voltage	VOH	IOL = 4,8mA	Vcc – 0.8	--	--	V
	VOL	IOL = 4,8mA	--	--	0.4	V
Input Leakage Current	ILK	VIH = VDD / VIL = GND	-1	--	1	uA
Sleep Current	ISP	--	--	0.5	1	mA
Sector Read Current	ISR	--	--	18	24	mA
Sector Write Current	ISW	--	--	25	30	mA

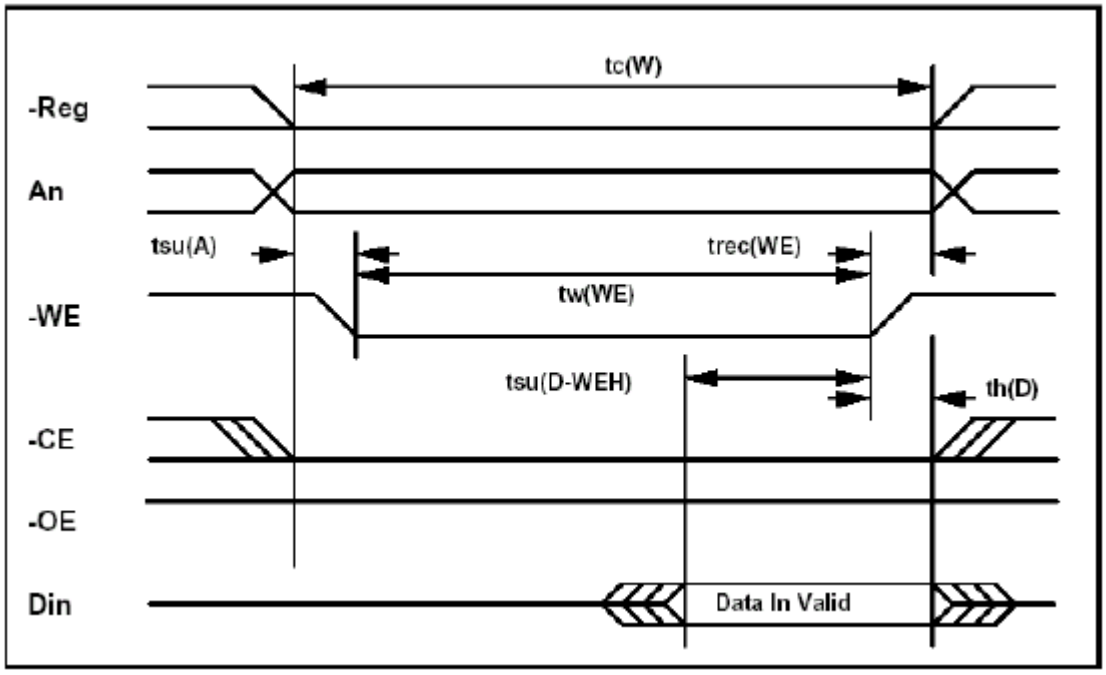
AC Characters

Attribute Memory Read Timing



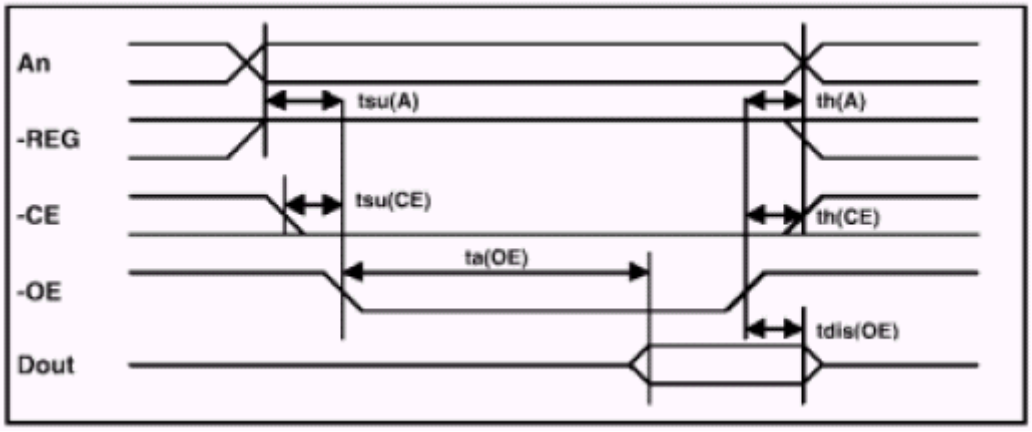
		250ns			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Read cycle time	TCR	250	–	–	ns
Address access time	ta(A)	–	–	250	ns
-CE access time	ta(CE)	–	–	250	ns
-OE access time	ta(OE)	–	–	125	ns
Output disable time(-CE)	tdis(CE)	–	–	100	ns
Output disable time(-OE)	tdis(OE)	–	–	100	ns
Output enable time(-CE)	ten(CE)	5	–	–	ns
Output enable time(-OE)	ten(OE)	5	–	–	ns
Data valid time(A)	tv(A)	0	–	–	ns
Address setup time	tsu(A)	30	–	–	ns

Attribute Memory Write Timing



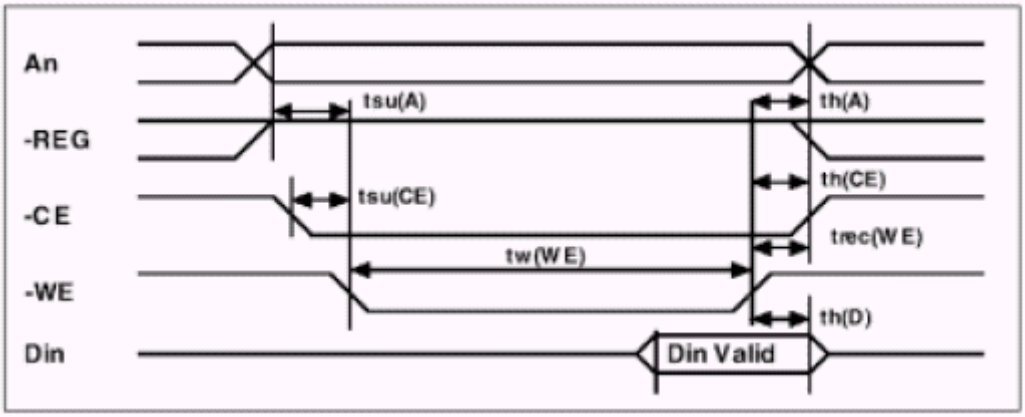
		250ns			
Parameter	Symbol	Min	Typ	Max	Unit
Write cycle time	tCW	250	—	—	ns
Write pulse time	tw(WE)	150	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
Data setup time (-WE)	tsu(D-WEH)	80	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write recover time	trec(WE)	30	—	—	ns

Common Memory Read Timing



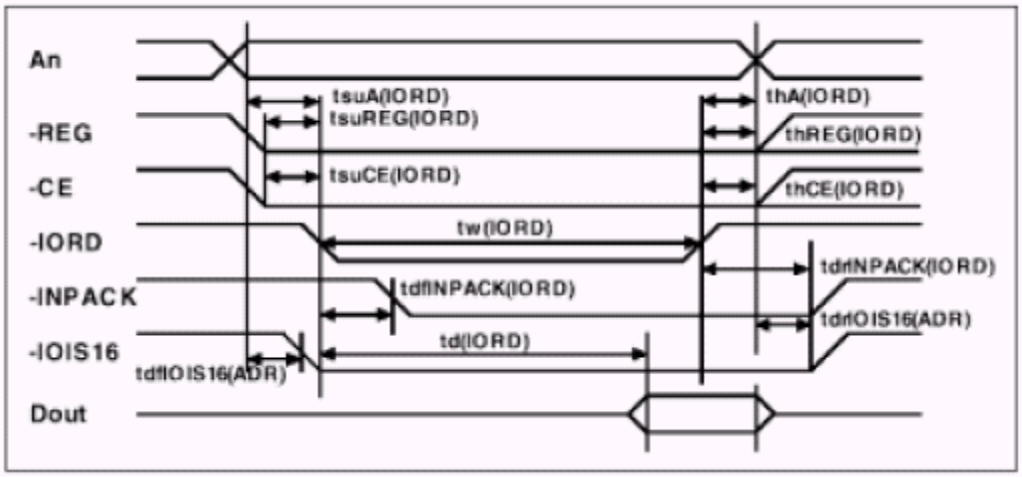
Parameter	Symbol	Min	Typ	Max	Unit
-OE access time	ta(OE)	–	–	125	ns
Output disable time (-OE)	tdis(OE)	–	–	100	ns
Address setup time	tsu(A)	30	–	–	ns
Address hold time	th(A)	20	–	–	ns
-CE setup time	tsu(CE)	0	–	–	ns
-CE hold time	th(CE)	20	–	–	ns

Common Memory Write Timing



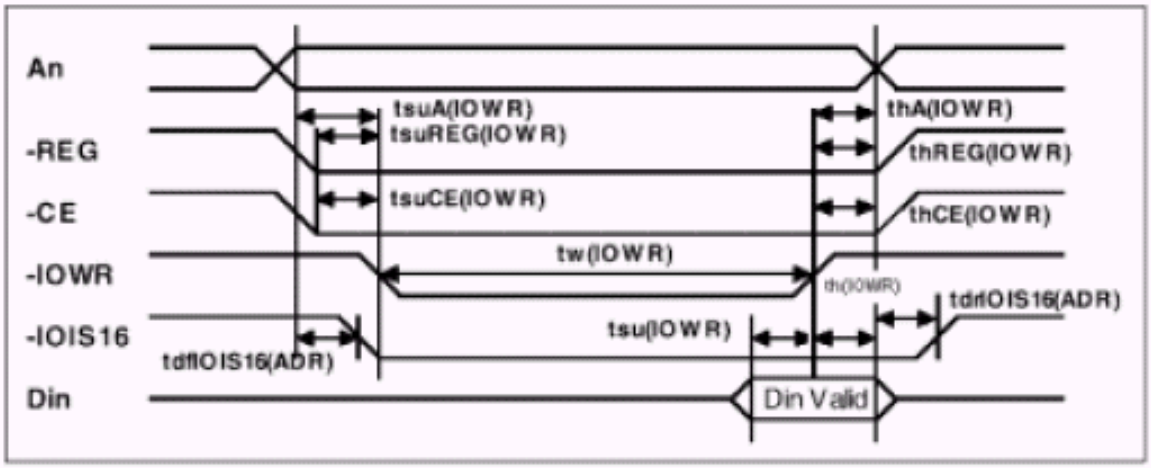
Parameter	Symbol	Min	Typ	Max	Unit
Data setup time (-WE)	tsu(D-WEH)	80	—	—	ns
Data hold time	th(D)	30	—	—	ns
Write pulse time	tw(WE)	150	—	—	ns
Address setup time	tsu(A)	30	—	—	ns
-CE setup time	tsu(CE)	0	—	—	ns
Write recover time	trec(WE)	30	—	—	ns
-CE hold following -WE	th(CE)	20	—	—	ns

I/O Input (Read) Timing



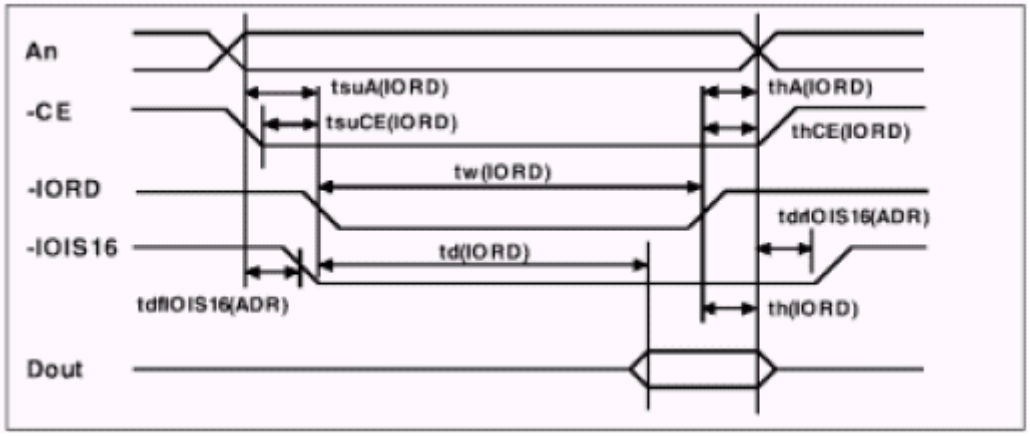
Parameter	Symbol	Min	Typ	Max	Unit
Data delay after –IORD	td(IORD)	—	—	100	ns
Data hold following –IORD	th(IORD)	0	—	—	ns
-IORD pulse width	tw(IORD)	165	—	—	ns
Address setup before -IORD	tsuA(IORD)	70	—	—	ns
Address hold following –IORD	thA(IORD)	20	—	—	ns
-CE setup before –IORD	tsuCE(IORD)	5	—	—	ns
-CE hold following –IORD	thCE(IORD)	20	—	—	ns
-REG setup before –IORD	tsuREG(IORD)	5	—	—	ns
-REG hold following –IORD	thREG(IORD)	0	—	—	ns
-INPACK delay failing from –IORD	tdfINPACK(IORD)	0	—	45	ns
-INPACK delay rising from –IORD	tdrINPACK(IORD)	—	—	45	ns
-IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
-IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

I/O Output (Write) Timing

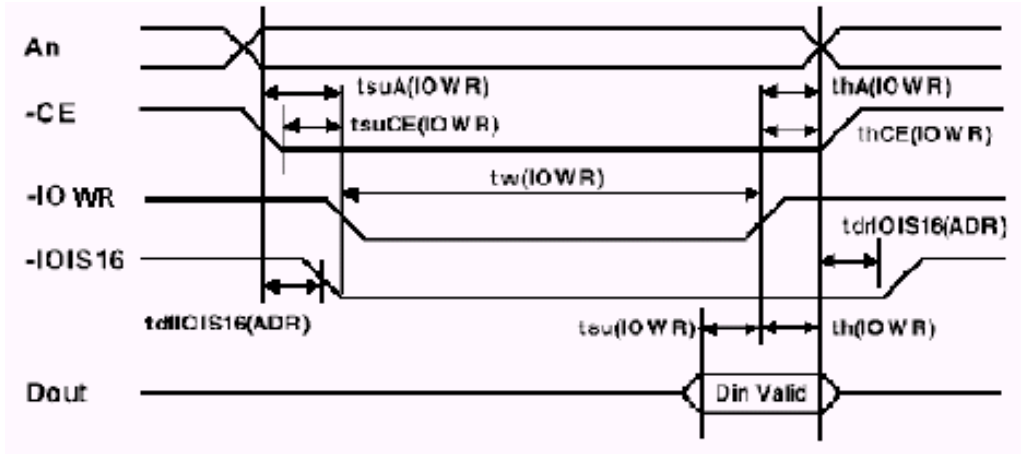


Parameter	Symbol	Min	Typ	Max	Unit
Data setup before –IOWR	tsu(IOWR)	60	—	—	ns
Data hold following –IOWR	th(IOWR)	30	—	—	ns
-IOWR pulse width	tw(IOWR)	165	—	—	ns
Address setup before –IOWR	tsuA(IOWR)	70	—	—	ns
Address hold following –IOWR	thA(IOWR)	20	—	—	ns
-CE setup before –IOWR	tsuCE(IOWR)	5	—	—	ns
-CE hold following –IOWR	thCE(IOWR)	20	—	—	ns
-REG setup before –IOWR	tsuREG(IOWR)	5	—	—	ns
-REG hold following –IOWR	thREG(IOWR)	0	—	—	ns
-IOIS16 delay falling from address	tdfIOIS16(ADR)	—	—	35	ns
-IOIS16 delay rising from address	tdrIOIS16(ADR)	—	—	35	ns

True IDE Mode I/O Timing



Input (Read) Timing

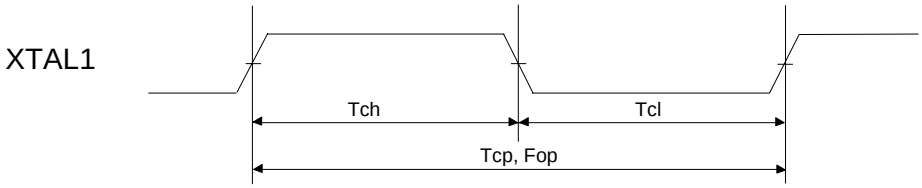


Output (Write) Timing

Parameter	Symbol	Supported	Unit
Data setup before IOWR (min)	tsu(IOWR)	20	ns
Data hold following IOWR (min)	Th(IOWR)	10	ns
Data delay after IORD (max)	Td(IORD)	50	ns
Data hold following IORD (min)	Th(IORD)	5	ns
IOWR/ IORD width time (min)	tw(IOWR/ IORD)	70	ns
Address setup before IOWR/IORD (min)	tsuA(IOWR/IORD)	15	ns
Address hold following IOWR/IORD (min)	thA(IOWR/IORD)	10	ns
CE setup before IOWR/IORD (min)	TsuCE(IOWR/IORD)	5	ns
CE hold following IOWR/IORD (min)	thCE(IOWR/IORD)	10	ns
IOIS16 delay falling from address (max)	tdfIOIS16(ADR)	35	ns
IOIS16 delay rising from address (max)	tsfIOIS16(ADR)	35	ns

Note: This timing applies only to modes 0, 1 and 2. For modes 3 and 4, the “IOIS16” signal is not valid.

Clock Input Timing

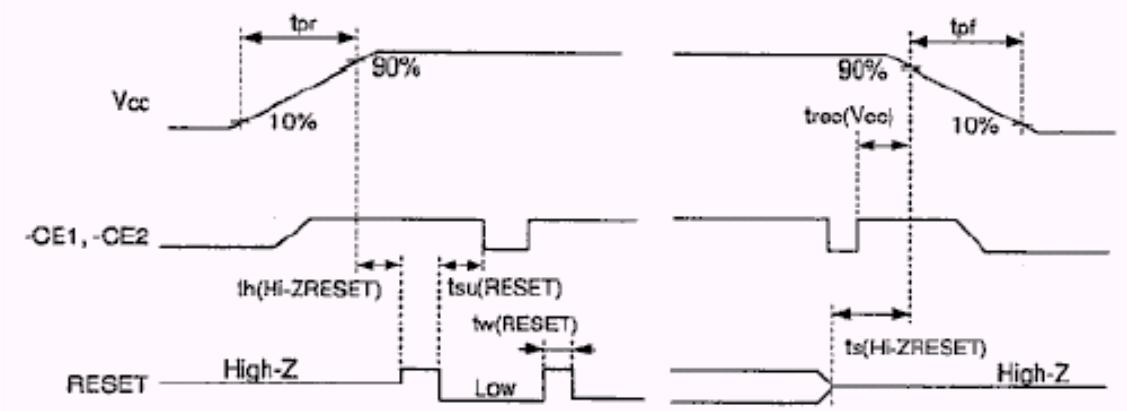


Parameter	Symbol	Min	Typ	Max	Unit
Operating Speed	Fop	0	28.4	40	MHz
Clock Period	Tcp	25	35	-	ns
Clock High	Tch	12.5	17.5	-	ns
Clock Low	Tcl	12.5	17.5	-	ns

Notes: 1. The clock may be stopped indefinitely in either state.

2. The Tcp specification is used as a reference in other specifications.

Hard Reset Timing



Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reset setup time	tsu(RESET)	100	—	—	ms	
-CE recover time	trec(VCC)	1	—	—	µs	
VCC rising up time	tpr	0.1	—	100	ms	
VCC falling down time	tpf	3	—	300	ms	
Reset pulse width	tw(RESET)	10	—	—	µs	
	th(Hi-ZRESET)	1	—	—	ms	
	ts(Hi-ZRESET)	0	—	—	ms	